

K9XXG08UXA

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Document Title

1G x 8 Bit / 2G x 8 Bit / 4G x 8 Bit NAND Flash Memory

Revision History

| <u>Revision No</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|--------------------|--|-------------------|---------------|
| 0.0 | 1. Initial issue | Nov. 09. 2005 | Advance |
| 0.1 | 1. Leaded part is eliminated 2. tRHW is defined | Jan. 10. 2006 | Preliminary |
| 1.0 | 1. Comment of "Addressing for program operation" is added (p.17) | Mar. 7. 2006 | Final |
| 1.1 | 1. 4GB DSP is added | July 18th 2006 | |

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1G x 8 Bit / 2G x 8 Bit / 4G x 8 Bit NAND Flash Memory

PRODUCT LIST

| Part Number | Vcc Range | Organization | PKG Type |
|--------------|--------------|--------------|-----------|
| K9K8G08U0A-Y | 2.70 ~ 3.60V | X8 | TSOP1 |
| K9WAG08U1A-Y | | | 52TLGA |
| K9WAG08U1A-I | | | TSOP1-DSP |
| K9NBG08U5A-P | | | |

FEATURES

- Voltage Supply
 - 2.70V ~ 3.60V
- Organization
 - Memory Cell Array : (1G + 32M) x 8bit
 - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
 - Page Program : (2K + 64)Byte
 - Block Erase : (128K + 4K)Byte
- Page Read Operation
 - Page Size : (2K + 64)Byte
 - Random Read : 25μs(Max.)
 - Serial Access : 25ns(Min.)
 - * K9NBG08U5A : 50ns(Min.)
- Fast Write Cycle Time
 - Page Program time : 200μs(Typ.)
 - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
 - Endurance : 100K Program/Erase Cycles(with 1bit/512Byte ECC)
 - Data Retention : 10 Years
- Command Driven Operation
- Intelligent Copy-Back with internal 1bit/528Byte EDC
- Unique ID for Copyright Protection
- Package :
 - K9K8G08U0A-PCB0/PIB0
 - 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
 - K9WAG08U1A-PCB0/PIB0
 - 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
 - K9WAG08U1A-ICB0/IIB0
 - 52 - Pin TLGA (12 x 17 / 1.0 mm pitch)
 - K9NBG08U5A-PCB0/PIB0
 - 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)

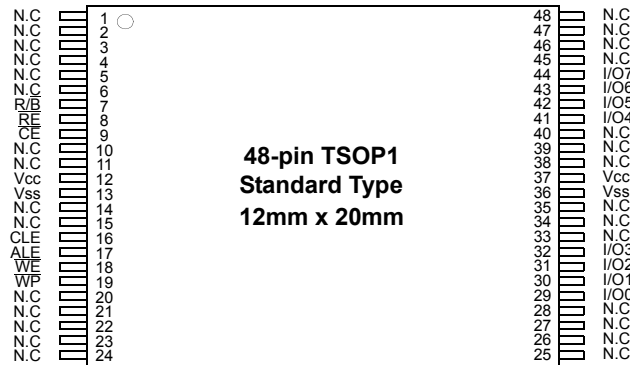
GENERAL DESCRIPTION

Offered in 1G x 8bit, the K9K8G08U0A is a 8G-bit NAND Flash Memory with spare 256M-bit. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 200μs on the (2K+64)Byte page and an erase operation can be performed in typical 1.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns(K9NBG08U5A : 50ns) cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9K8G08U0A's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9K8G08U0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

An ultra high density solution having two 8Gb stacked with two chip selects is also available in standard TSOP1 package and another ultra high density solution having two 16Gb TSOP1 package stacked with four chip selects is also available in TSOP1-DSP.

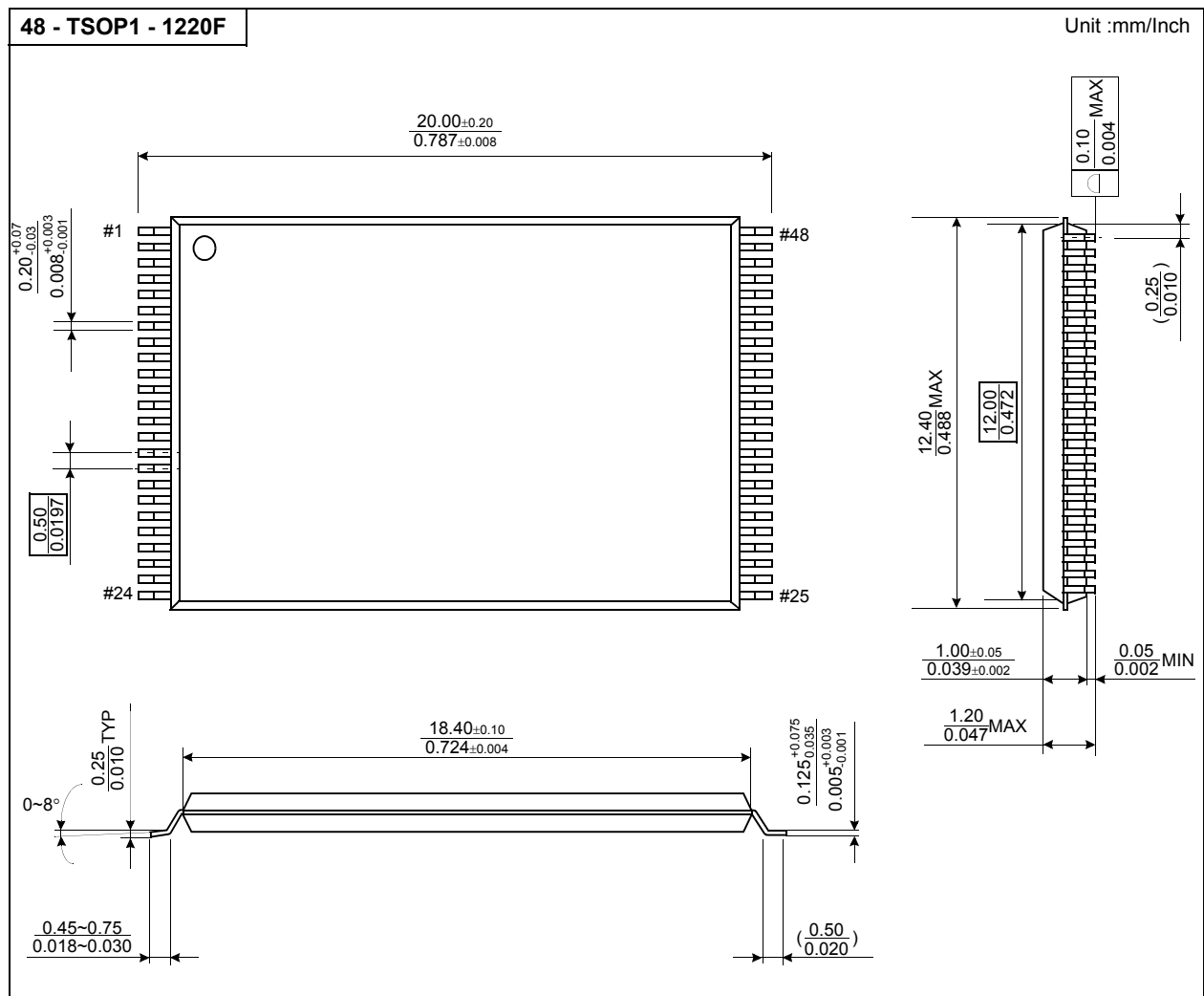
PIN CONFIGURATION (TSOP1)

K9K8G08U0A-PCB0/PIB0



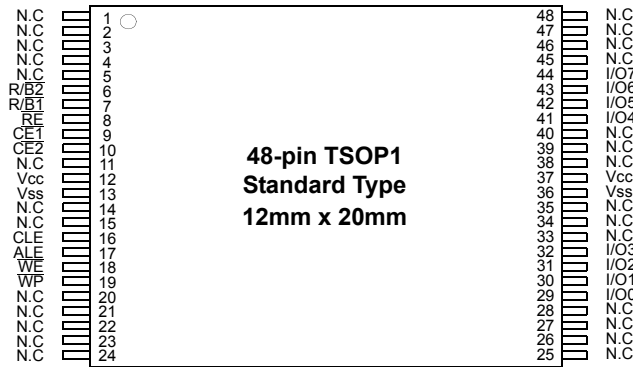
PACKAGE DIMENSIONS

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



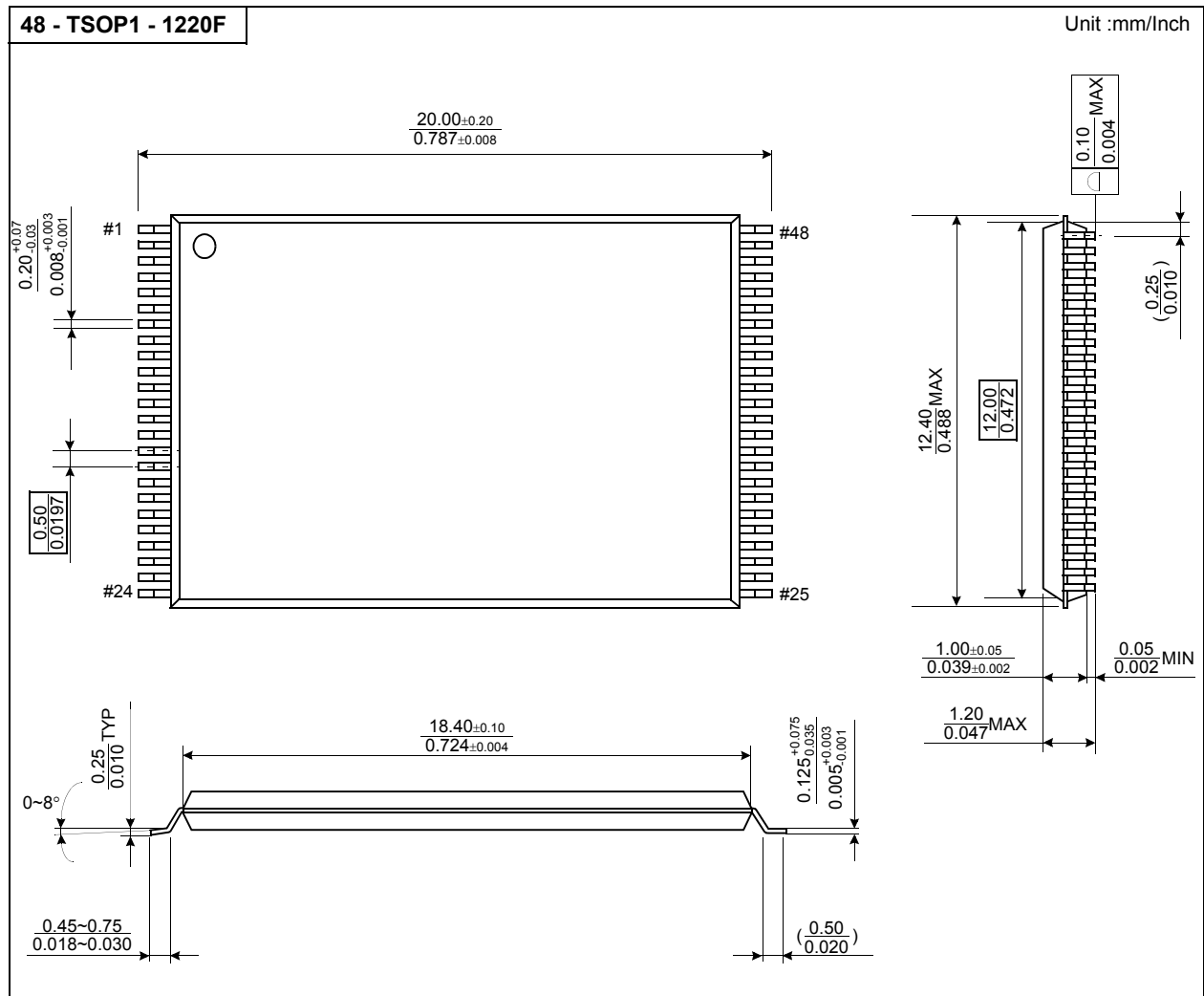
PIN CONFIGURATION (TSOP1)

K9WAG08U1A-PCB0/PIB0

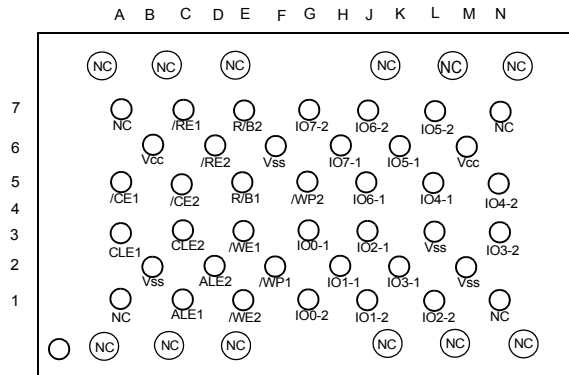


PACKAGE DIMENSIONS

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

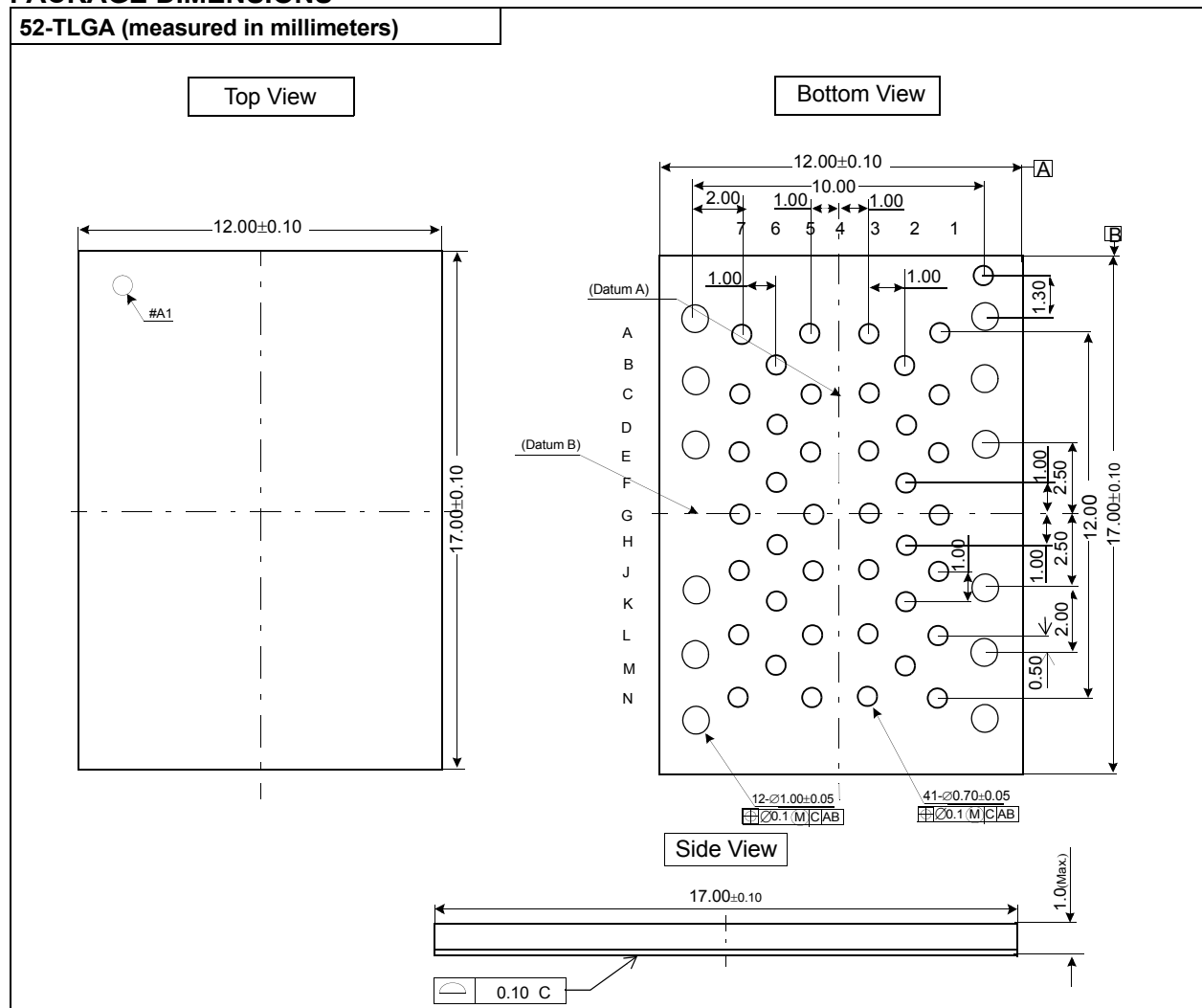


K9WAG08U1A - ICB0 / IIB0



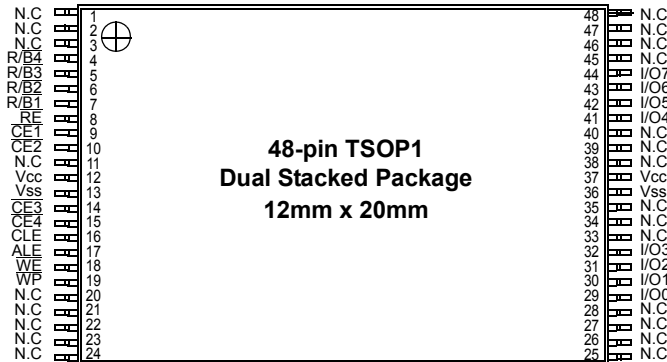
PACKAGE DIMENSIONS

52-TLGA (measured in millimeters)



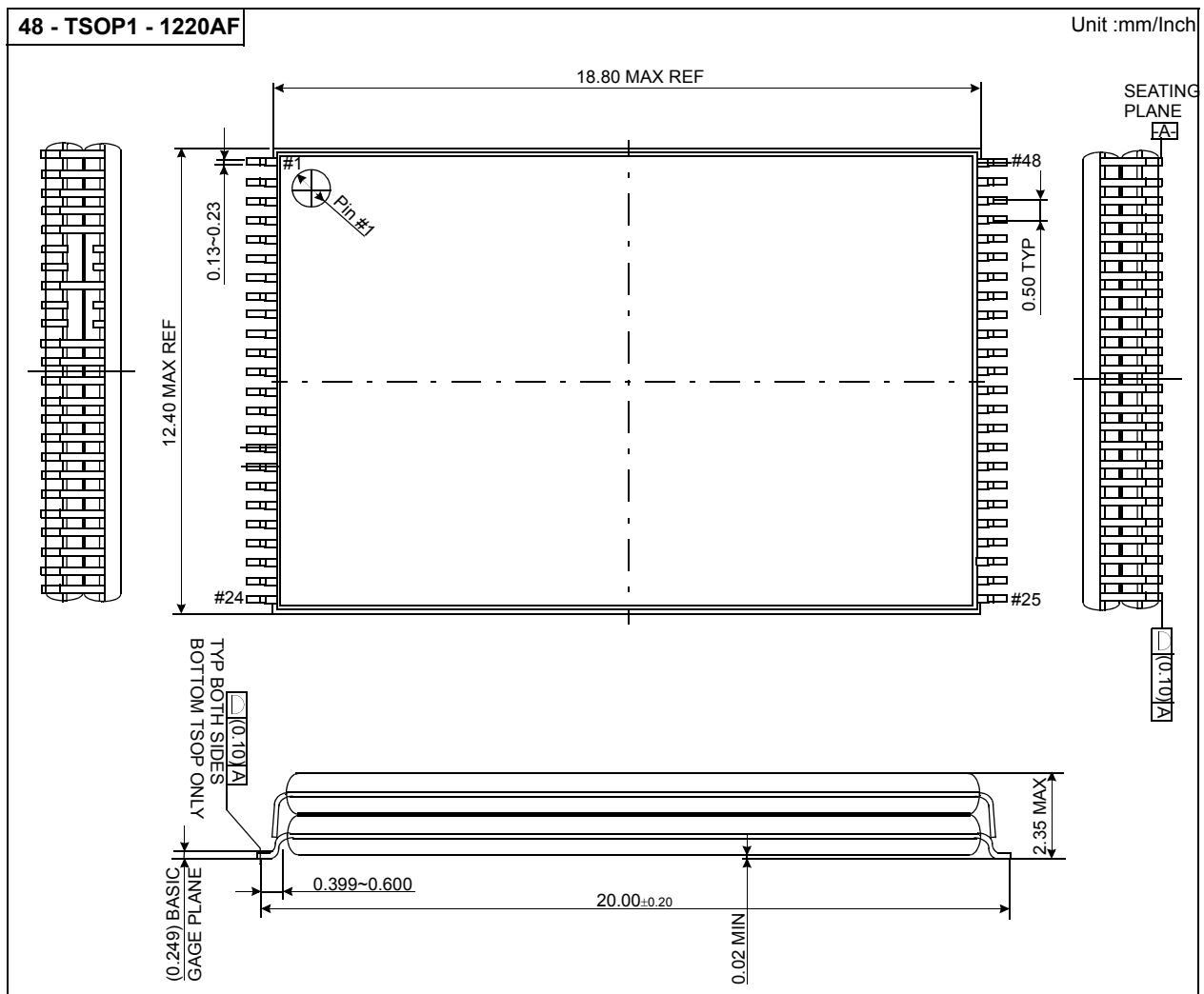
PIN CONFIGURATION (TSOP1-DSP)

K9NBG08U5A-PCB0/PIB0



PACKAGE DIMENSIONS

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



PIN DESCRIPTION

| Pin Name | Pin Function |
|-------------------------------------|---|
| I/O ₀ ~ I/O ₇ | DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. |
| CLE | COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the \overline{WE} signal. |
| ALE | ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of \overline{WE} with ALE high. |
| \overline{CE} / $\overline{CE1}$ | CHIP ENABLE The \overline{CE} / $\overline{CE1}$ input is the device selection control. When the device is in the Busy state, \overline{CE} / $\overline{CE1}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding \overline{CE} / $\overline{CE1}$ control during read operation, refer to 'Page Read' section of Device operation. |
| $\overline{CE2}$ | CHIP ENABLE The $\overline{CE2}$ input enables the second K9K8G08U0A |
| \overline{RE} | READ ENABLE The \overline{RE} input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of \overline{RE} which also increments the internal column address counter by one. |
| \overline{WE} | WRITE ENABLE The \overline{WE} input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the \overline{WE} pulse. |
| \overline{WP} | WRITE PROTECT The \overline{WP} pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low. |
| $R\overline{B}$ / $R\overline{B1}$ | READY/BUSY OUTPUT The $R\overline{B}$ / $R\overline{B1}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. |
| Vcc | POWER Vcc is the power supply for device. |
| Vss | GROUND |
| N.C | NO CONNECTION Lead is not internally connected. |

NOTE : Connect all Vcc and Vss pins of each device to common power supply outputs.

Do not leave Vcc or Vss disconnected.

There are two \overline{CE} pins ($\overline{CE1}$ & $\overline{CE2}$) in the K9WAG08U1A and four \overline{CE} pins ($\overline{CE1}$ & $\overline{CE2}$ & $\overline{CE3}$ & $\overline{CE4}$) in the K9NBG08U5A.

There are two $R\overline{B}$ pins ($R\overline{B1}$ & $R\overline{B2}$) in the K9WAG08U1A and four $R\overline{B}$ pins ($R\overline{B1}$ & $R\overline{B2}$ & $R\overline{B3}$ & $R\overline{B4}$) in the K9NBG08U5A.

Figure 1. K9K8G08U0A Functional Block Diagram

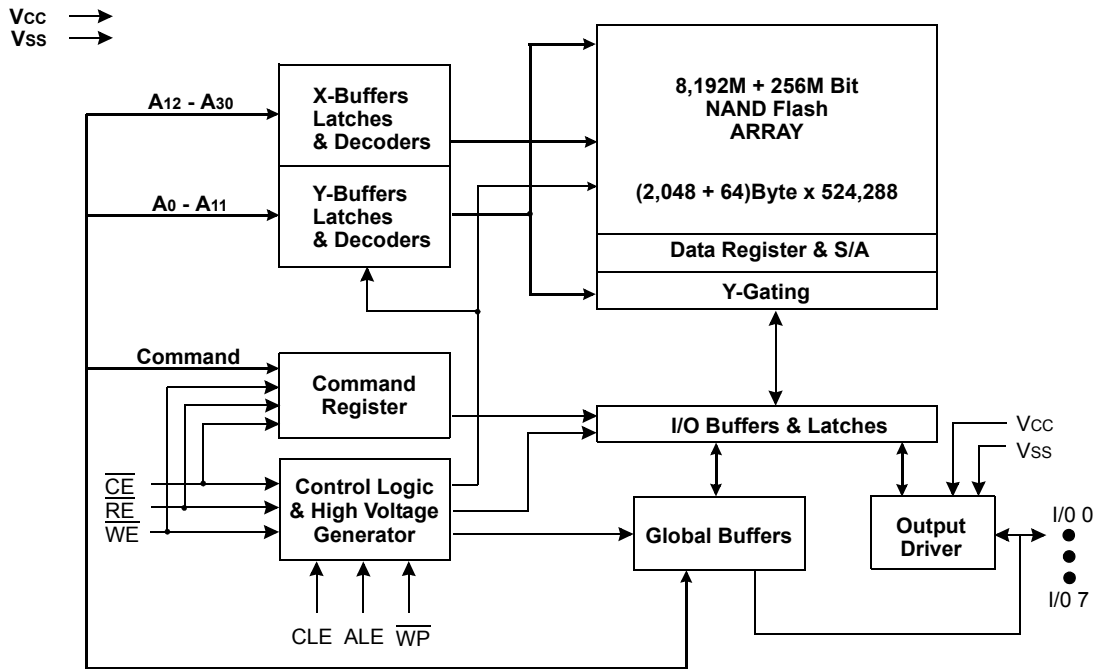
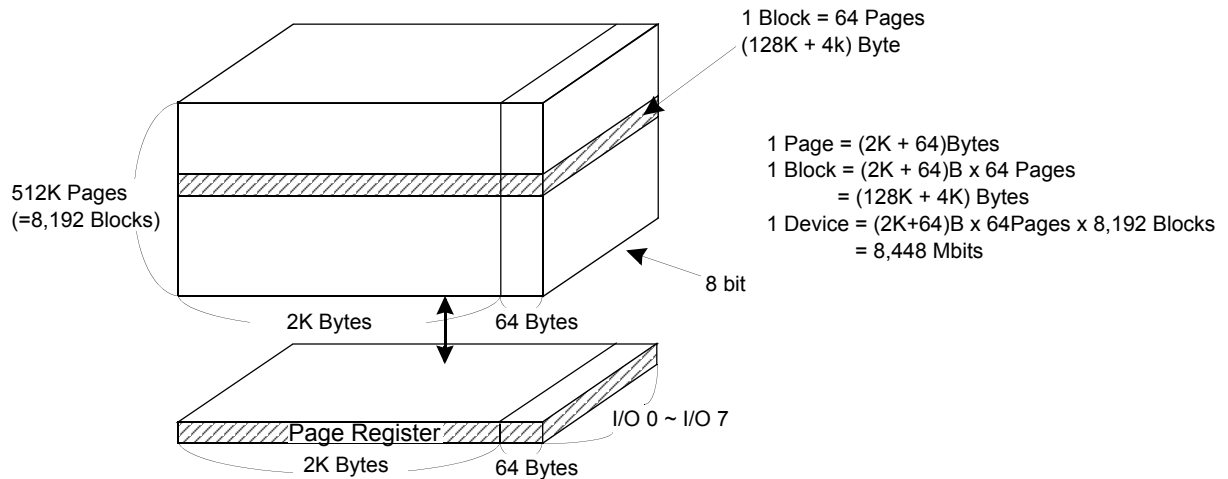


Figure 2. K9K8G08U0A Array Organization



| | I/O 0 | I/O 1 | I/O 2 | I/O 3 | I/O 4 | I/O 5 | I/O 6 | I/O 7 | |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|----------------|
| 1st Cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | Column Address |
| 2nd Cycle | A8 | A9 | A10 | A11 | *L | *L | *L | *L | Column Address |
| 3rd Cycle | A12 | A13 | A14 | A15 | A16 | A17 | A18 | A19 | Row Address |
| 4th Cycle | A20 | A21 | A22 | A23 | A24 | A25 | A26 | A27 | Row Address |
| 5th Cycle | A28 | A29 | A30 | *L | *L | *L | *L | *L | Row Address |

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than required.

Product Introduction

The K9K8G08U0A is a 8,448Mbit(8,858,370,048 bit) memory organized as 524,288 rows(pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. Total 1,081,344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 8,192 separately erasable 128K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9K8G08U0A.

The K9K8G08U0A has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 1056M byte physical space requires 31 addresses, thereby requiring five cycles for addressing : 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9K8G08U0A.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

The K9WAG08U1A is composed of two K9K8G08U0A chips which are selected separately by each $\overline{CE1}$ and $\overline{CE2}$ and the K9NBG08U5A is composed of four K9K8G08U0A chips which are selected separately by each $\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$. Therefore, in terms of each CE, the basic operations of K9WAG08U0A and K9NBG08U5A are same with K9K8G08U0A except some AC/DC characteristics.

Table 1. Command Sets

| Function | 1st Cycle | 2nd Cycle | Acceptable Command during Busy |
|--|-----------|-----------|--------------------------------|
| Read | 00h | 30h | |
| Read for Copy Back | 00h | 35h | |
| Read ID | 90h | - | |
| Reset | FFh | - | O |
| Page Program | 80h | 10h | |
| Two-Plane Page Program ⁽⁴⁾ | 80h---11h | 81h---10h | |
| Copy-Back Program | 85h | 10h | |
| Two-Plane Copy-Back Program ⁽⁴⁾ | 85h---11h | 81h---10h | |
| Block Erase | 60h | D0h | |
| Two-Plane Block Erase | 60h---60h | D0h | |
| Random Data Input ⁽¹⁾ | 85h | - | |
| Random Data Output ⁽¹⁾ | 05h | E0h | |
| Read Status | 70h | | O |
| Read EDC Status ⁽²⁾ | 7Bh | | O |
| Chip1 Status ⁽³⁾ | F1h | | O |
| Chip2 Status ⁽³⁾ | F2h | | O |

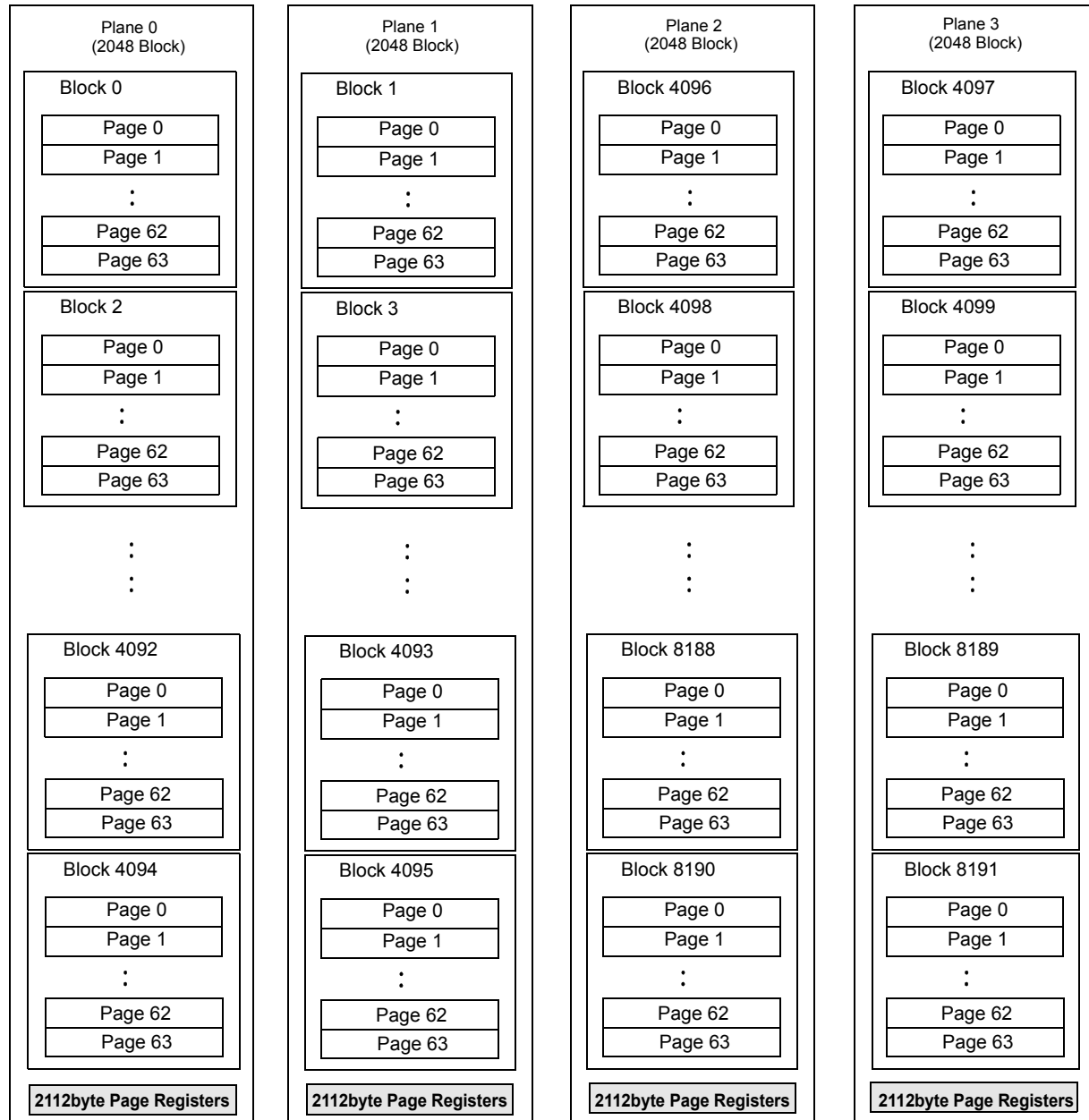
- NOTE :** 1. Random Data Input/Output can be executed in a page.
 2. Read EDC Status is only available on Copy Back operation.
 3. Interleave-operation between two chips is allowed.
 It's prohibited to use F1h and F2h commands for other operations except interleave-operation.
 4. Any command between 11h and 81h is prohibited except 70h, F1h, F2h and FFh .

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

Memory Map

K9K8G08U0A is arranged in four 2Gb memory planes. Each plane contains 2,048 blocks and 2112 byte page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that two-plane program/erase operations can be executed by dividing the memory array into plane 0~1 or plane 2~3 separately.

For example, two-plane program/erase operation into plane 0 and plane 2 is prohibited. That is to say, two-plane program/erase operation into plane 0 and plane 1 or into plane 2 and plane 3 is allowed



ABSOLUTE MAXIMUM RATINGS

| Parameter | | Symbol | Rating | Unit |
|------------------------------------|-----------------|-------------------|--------------------------------------|------|
| Voltage on any pin relative to VSS | | V _{CC} | -0.6 to +4.6 | V |
| | | V _{IN} | -0.6 to +4.6 | |
| | | V _{I/O} | -0.6 to V _{CC} +0.3 (<4.6V) | |
| Temperature Under Bias | K9XXG08UXA-XCB0 | T _{BIAS} | -10 to +125 | °C |
| | K9XXG08UXA-XIB0 | | -40 to +125 | |
| Storage Temperature | K9XXG08UXA-XCB0 | T _{STG} | -65 to +150 | °C |
| | K9XXG08UXA-XIB0 | | | |
| Short Circuit Current | | I _{OS} | 5 | mA |

NOTE :

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9XXG08UXA-XCB0 :T_A=0 to 70°C, K9XXG08UXA-XIB0:T_A=-40 to 85°C)

| Parameter | Symbol | Min | Typ. | Max | Unit |
|----------------|-----------------|-----|------|-----|------|
| Supply Voltage | V _{CC} | 2.7 | 3.3 | 3.6 | V |
| Supply Voltage | V _{SS} | 0 | 0 | 0 | V |

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|------------------------------|----------------------------------|---|---------------------|-----|----------------------|------|
| Operating Current | Page Read with Serial Access | I _{CC1} | t _{RC} =25ns(K9NBG08U5A: 50ns) CE=V _{IL} , I _{OUT} =0mA | - | 25 | 35 | mA |
| | Program | I _{CC2} | - | | | | |
| | Erase | I _{CC3} | - | | | | |
| Stand-by Current(TTL) | | I _{SB1} | CE=V _{IH} , WP=0V/V _{CC} | - | - | 1 | μA |
| Stand-by Current(CMOS) | | I _{SB2} | CE=V _{CC} -0.2, WP=0V/V _{CC} | - | 20 | 100 | |
| Input Leakage Current | | I _{LI} | V _{IN} =0 to V _{CC} (max) | - | - | ±20 | |
| Output Leakage Current | | I _{LO} | V _{OUT} =0 to V _{CC} (max) | - | - | ±20 | |
| Input High Voltage | | V _{IH} (¹) | - | 0.8xV _{CC} | - | V _{CC} +0.3 | V |
| Input Low Voltage, All inputs | | V _{IL} (¹) | - | -0.3 | - | 0.2xV _{CC} | |
| Output High Voltage Level | | V _{OH} | I _{OH} =-400μA | 2.4 | - | - | |
| Output Low Voltage Level | | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | mA |
| Output Low Current(R/B) | | I _{OL} (R/B) | V _{OL} =0.4V | 8 | 10 | - | |

- NOTE :**
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.
 2. Typical value is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
 3. The typical value of the K9WAG08U1A's I_{SB2} is 40μA and the maximum value is 200μA.
 4. The typical value of the K9NBG08U5A's I_{SB2} is 80μA and the maximum value is 400μA.
 5. The maximum value of K9WAG08U1A-P's I_{LI} and I_{LO} is ±40μA, the maximum value of K9WAG08U1A-I's I_{LI} and I_{LO} is ±20μA.
 6. The maximum value of K9NBG08U5A's I_{LI} and I_{LO} is ±80μA.

VALID BLOCK

| Parameter | Symbol | Min | Typ. | Max | Unit |
|------------|--------|---------|------|---------|--------|
| K9K8G08U0A | NvB | 8,032 | - | 8,192 | Blocks |
| K9WAG08U1A | NvB | 16,064* | - | 16,384* | Blocks |
| K9NBG08U5A | NvB | 32,128* | | 32,768* | Blocks |

NOTE :

- The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
 - The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.
 - The number of valid block is on the basis of single plane operations, and this may be decreased with two plane operations.
- * : Each K9K8G08U0A chip in the K9WAG08U1A and K9NBG08U5A has Maximun 160 invalid blocks.

AC TEST CONDITION

(K9XXG08UXA-XCB0: TA=0 to 70°C, K9XXG08UXA-XIB0:TA=-40 to 85°C ,K9XXG08UXA: Vcc=2.7V~3.6V unless otherwise noted)

| Parameter | K9XXG08UXA |
|--------------------------------|--|
| Input Pulse Levels | 0V to Vcc |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | Vcc/2 |
| Output Load | 1 TTL GATE and CL=50pF (K9K8G08U0A-P/K9WAG08U1A-I) |
| | 1 TTL GATE and CL=30pF (K9WAG08U1A-P) |
| | 1 TTL GATE and CL=30pF (K9NBG08U5A-P) |

CAPACITANCE(TA=25°C, VCC=3.3V, f=1.0MHz)

| Item | Symbol | Test Condition | Min | Max | | | Unit |
|----------------------|------------------|---------------------|-----|------------|-------------|------------|------|
| | | | | K9K8G08U0A | K9WAG08U1A* | K9NBG08U5A | |
| Input/Output Capaci- | C _{I/O} | V _{IL} =0V | - | 20 | 40 | 80 | pF |
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 20 | 40 | 80 | pF |

NOTE : Capacitance is periodically sampled and not 100% tested.
 K9WAG08U1A-IXB0's capacitance(I/O, Input) is 20pF.

MODE SELECTION

| CLE | ALE | CE | WE | RE | WP | Mode | |
|-----|------------------|----|----|----|-----------------------|----------------------|-----------------------|
| H | L | L | | H | X | Read Mode | Command Input |
| L | H | L | | H | X | | Address Input(5clock) |
| H | L | L | | H | H | Write Mode | Command Input |
| L | H | L | | H | H | | Address Input(5clock) |
| L | L | L | | H | H | Data Input | |
| L | L | L | H | | X | Data Output | |
| X | X | X | X | H | X | During Read(Busy) | |
| X | X | X | X | X | H | During Program(Busy) | |
| X | X | X | X | X | H | During Erase(Busy) | |
| X | X ⁽¹⁾ | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/Vcc ⁽²⁾ | Stand-by | |

NOTE : 1. X can be V_{IL} or V_{IH}.
 2. WP should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------------|-----|-----|-----|--------|
| Program Time | t _{PROG} | - | 200 | 700 | μs |
| Dummy Busy Time for Two-Plane Page Program | t _{DBSY} | - | 0.5 | 1 | μs |
| Number of Partial Program Cycles | Nop | - | - | 4 | cycles |
| Block Erase Time | t _{BERS} | - | 1.5 | 2 | ms |

NOTE : 1. Typical value is measured at V_{cc}=3.3V, T_A=25°C. Not 100% tested.

2. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V V_{cc} and 25°C temperature.

AC Timing Characteristics for Command / Address / Data Input

| Parameter | Symbol | Min | | Max | | Unit |
|---------------------------------------|---------------------------------|------------|------------|------------|------------|------|
| | | K9NBG08U5A | K9K8G08U0A | K9NBG08U5A | K9K8G08U0A | |
| | | | K9WAG08U1A | | K9WAG08U1A | |
| CLE Setup Time | t _{CLS} ⁽¹⁾ | 25 | 12 | - | - | ns |
| CLE Hold Time | t _{CLH} | 10 | 5 | - | - | ns |
| $\overline{\text{CE}}$ Setup Time | t _{CS} ⁽¹⁾ | 35 | 20 | - | - | ns |
| $\overline{\text{CE}}$ Hold Time | t _{CH} | 10 | 5 | - | - | ns |
| $\overline{\text{WE}}$ Pulse Width | t _{WP} | 25 | 12 | - | - | ns |
| ALE Setup Time | t _{ALS} ⁽¹⁾ | 25 | 12 | - | - | ns |
| ALE Hold Time | t _{ALH} | 10 | 5 | - | - | ns |
| Data Setup Time | t _{DS} ⁽¹⁾ | 20 | 12 | - | - | ns |
| Data Hold Time | t _{DH} | 10 | 5 | - | - | ns |
| Write Cycle Time | t _{WC} | 45 | 25 | - | - | ns |
| $\overline{\text{WE}}$ High Hold Time | t _{WH} | 15 | 10 | - | - | ns |
| Address to Data Loading Time | t _{ADL} ⁽²⁾ | 70 | 70 | - | - | ns |

NOTES : 1. The transition of the corresponding control pins must occur only once while $\overline{\text{WE}}$ is held low

2. t_{ADL} is the time from the $\overline{\text{WE}}$ rising edge of final address cycle to the $\overline{\text{WE}}$ rising edge of first data cycle

AC Characteristics for Operation

| Parameter | Symbol | Min | | Max | | Unit |
|---|-------------------|------------|------------|-------------------------|-------------------------|------|
| | | K9NBG08U5A | K9K8G08U0A | K9NBG08U5A | K9K8G08U0A | |
| | | | K9WAG08U1A | | K9WAG08U1A | |
| Data Transfer from Cell to Register | t _R | | - | 20 | 20 | μs |
| ALE to \overline{RE} Delay | t _{AR} | 10 | 10 | | - | ns |
| CLE to \overline{RE} Delay | t _{CLR} | 10 | 10 | | - | ns |
| Ready to \overline{RE} Low | t _{RR} | 20 | 20 | | - | ns |
| \overline{RE} Pulse Width | t _{RP} | 25 | 12 | | - | ns |
| WE High to Busy | t _{WB} | - | - | 100 | 100 | ns |
| Read Cycle Time | t _{RC} | 50 | 25 | - | - | ns |
| \overline{RE} Access Time | t _{REA} | - | - | 30 | 20 | ns |
| \overline{CE} Access Time | t _{CEA} | - | - | 45 | 25 | ns |
| \overline{RE} High to Output Hi-Z | t _{RHZ} | - | - | 100 | 100 | ns |
| \overline{CE} High to Output Hi-Z | t _{CHZ} | - | - | 30 | 30 | ns |
| \overline{RE} High to Output hold | t _{RHOH} | 15 | 15 | - | - | ns |
| \overline{RE} Low to Output hold | t _{RLOH} | - | 5 | - | - | ns |
| \overline{CE} High to Output hold | t _{COH} | 15 | 15 | - | - | ns |
| \overline{RE} High Hold Time | t _{REH} | 15 | 10 | - | - | ns |
| Output Hi-Z to \overline{RE} Low | t _{IR} | 0 | 0 | - | - | ns |
| \overline{RE} High to \overline{WE} Low | t _{RHW} | 100 | 100 | - | - | ns |
| \overline{WE} High to \overline{RE} Low | t _{WHR} | 60 | 60 | - | - | ns |
| Device Resetting Time(Read/Program/Erase) | t _{RST} | - | - | 5/10/500 ⁽¹⁾ | 5/10/500 ⁽¹⁾ | μs |

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original initial invalid block information is prohibited.

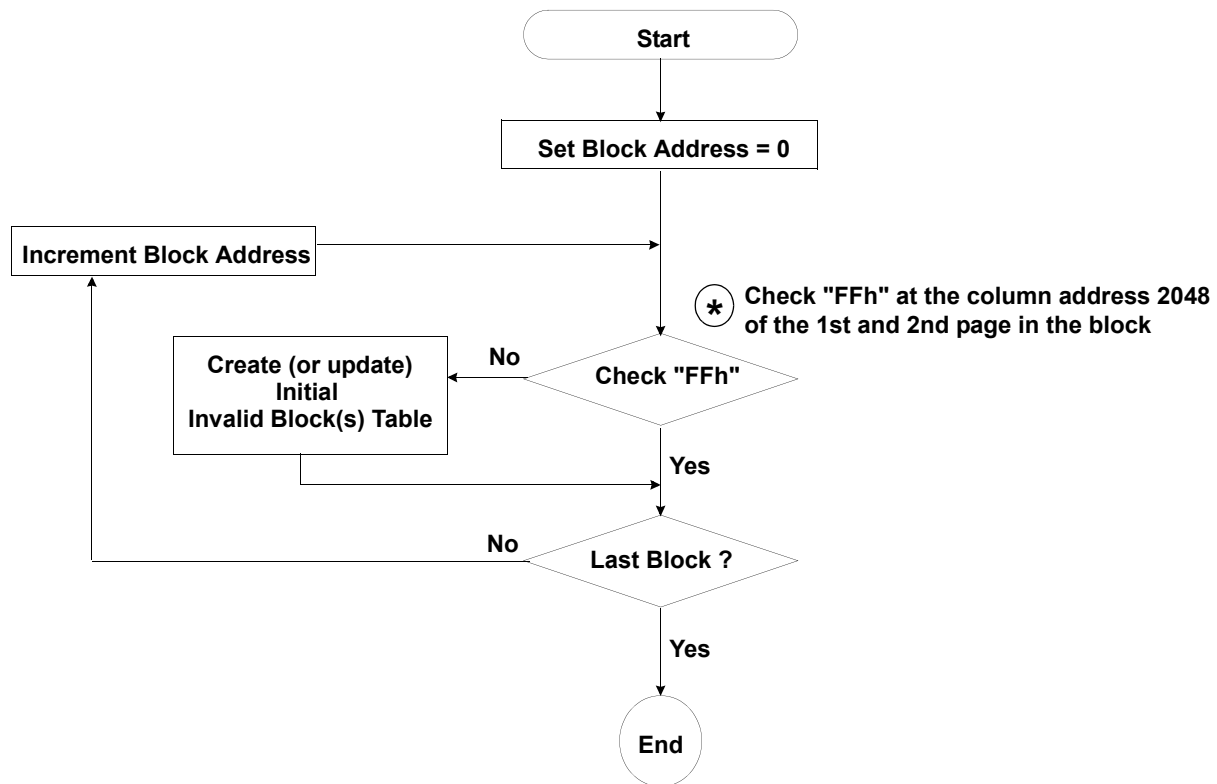


Figure 3. Flow chart to create initial invalid block table.

NAND Flash Technical Notes (Continued)

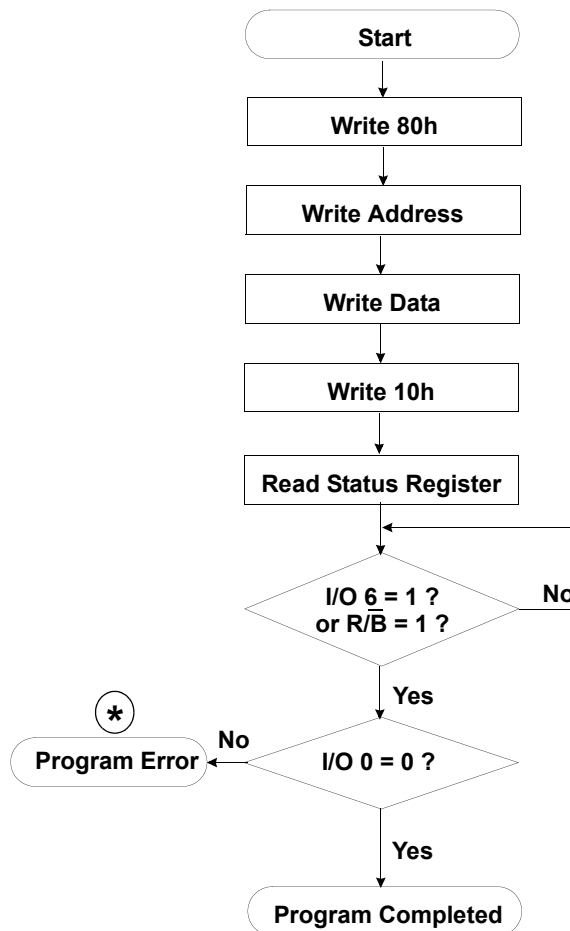
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

| Failure Mode | | Detection and Countermeasure sequence |
|--------------|--------------------|---|
| Write | Erase Failure | Status Read after Erase --> Block Replacement |
| | Program Failure | Status Read after Program --> Block Replacement |
| Read | Single Bit Failure | Verify ECC -> ECC Correction |

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

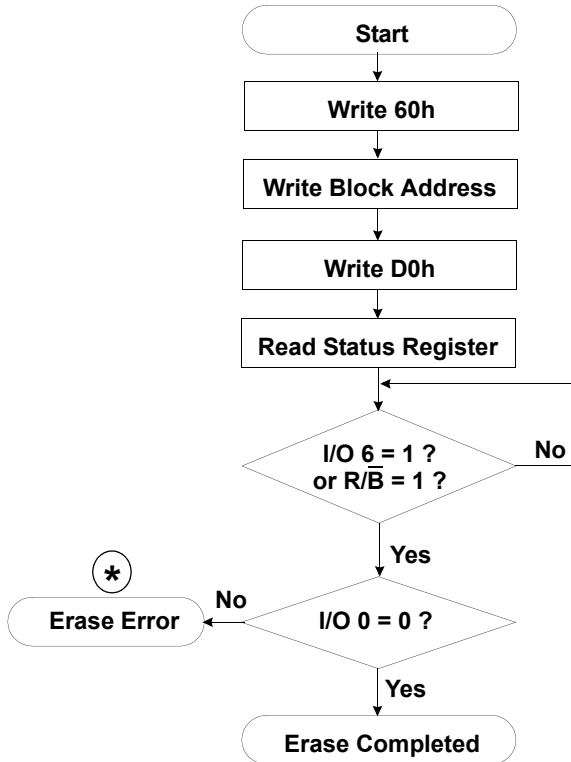
Program Flow Chart



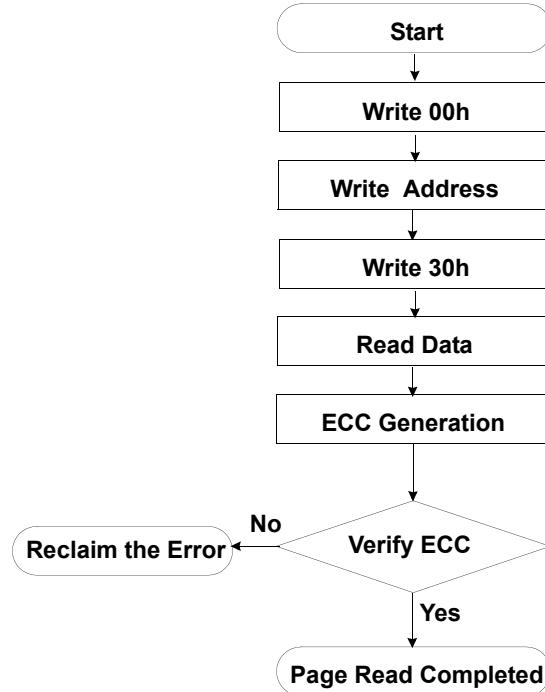
***** : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes (Continued)

Erase Flow Chart

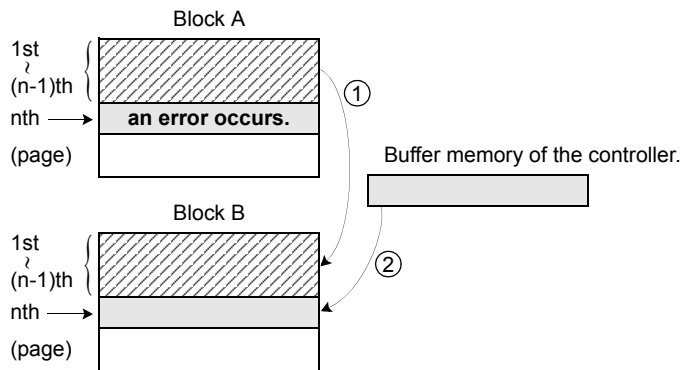


Read Flow Chart



* : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



- * Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
- * Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
- * Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
- * Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes (Continued)

Copy-Back Operation with EDC & Sector Definition for EDC

Generally, copy-back program is very powerful to move data stored in a page without utilizing any external memory. But, if the source page has one bit error due to charge loss or charge gain, then without EDC, the copy-back program operation could also accumulate bit errors.

K9K8G08U0A supports copy-back with EDC to prevent cumulative bit errors. To make EDC valid, the page program operation should be performed on either whole page(2112byte) or sector(528byte). **Modifying the data of a sector by Random Data Input before Copy-Back Program must be performed for the whole sector and is allowed only once per each sector. Any partial modification smaller than a sector corrupts the on-chip EDC codes.**

A 2,112-byte page is composed of 4 sectors of 528-byte and each 528-byte sector is composed of 512-byte main area and 16-byte spare area.

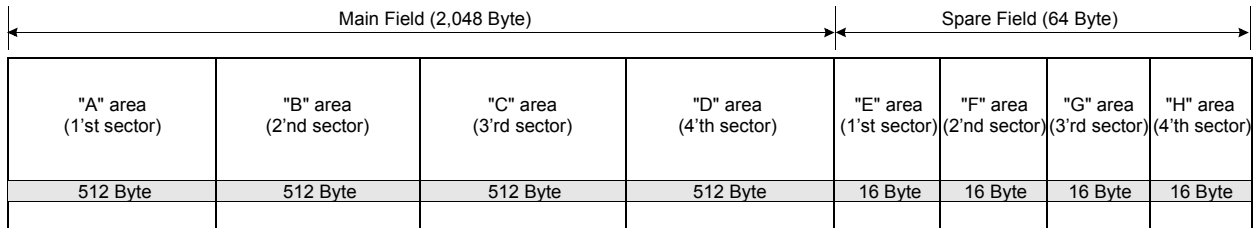
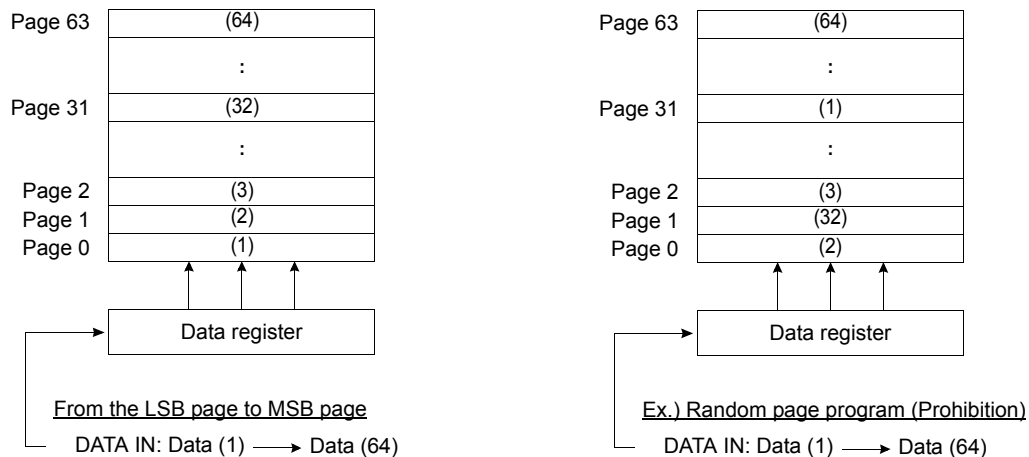


Table 2. Definition of the 528-Byte Sector

| Sector | Main Field (Column 0~2,047) | | Spare Field (Column 2,048~2,111) | |
|----------------------|-----------------------------|----------------|----------------------------------|----------------|
| | Area Name | Column Address | Area Name | Column Address |
| 1'st 528-Byte Sector | "A" | 0 ~ 511 | "E" | 2,048 ~ 2,063 |
| 2'nd 528-Byte Sector | "B" | 512 ~ 1,023 | "F" | 2,064 ~ 2,079 |
| 3'rd 528-Byte Sector | "C" | 1,024 ~ 1,535 | "G" | 2,080 ~ 2,095 |
| 4'th 528-Byte Sector | "D" | 1,536 ~ 2,047 | "H" | 2,096 ~ 2,111 |

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.



Interleave Page Program

K9K8G08U0A is composed of two K9F4G08U0As. K9K8G08U0A provides interleaving operation between two K9F4G08U0As.

This interleaving page program improves the system throughput almost twice compared to non-interleaving page program.

At first, the host issues page program command to one of the K9F4G08U0A chips, say K9F4G08U0A(chip #1). Due to this K9K8G08U0A goes into busy state. During this time, K9F4G08U0A(chip #2) is in ready state. So it can execute the page program command issued by the host.

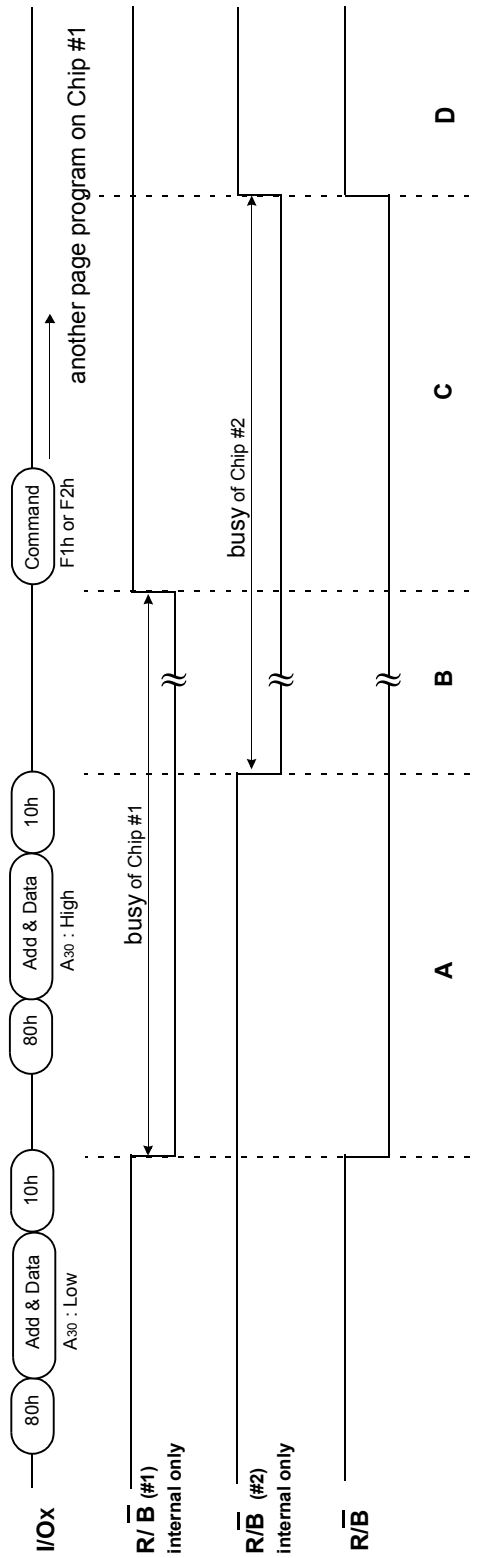
After the execution of page program by K9F4G08U0A(chip #1), it can execute another page program regardless of the K9F4G08U0A(chip #2). Before that the host needs to check the status of K9F4G08U0A(chip #1) by issuing F1h command. Only when the status of K9F4G08U0A(chip #1) becomes ready status, host can issue another page program command. If the K9F4G08U0A(chip #1) is in busy state, the host has to wait for the K9F4G08U0A(chip #1) to get into ready state.

Similarly, K9F4G08U0A chip(chip #2) can execute another page program after the completion of the previous program. The host can monitor the status of K9F4G08U0A(chip #2) by issuing F2h command. When the K9F4G08U0A(chip #2) shows ready state, host can issue another page program command to K9F4G08U0A(chip #2).

This interleaving algorithm improves the system throughput almost twice. The host can issue page program command to each chip individually. This reduces the time lag for the completion of operation.

NOTES : During interleave operations, 70h command is prohibited.

Interleave Page Program



State A : Chip #1 is executing a page program operation and chip #2 is in ready state. So the host can issue a page program command to chip #2.

State B : Both chip #1 and chip #2 are executing page program operation.

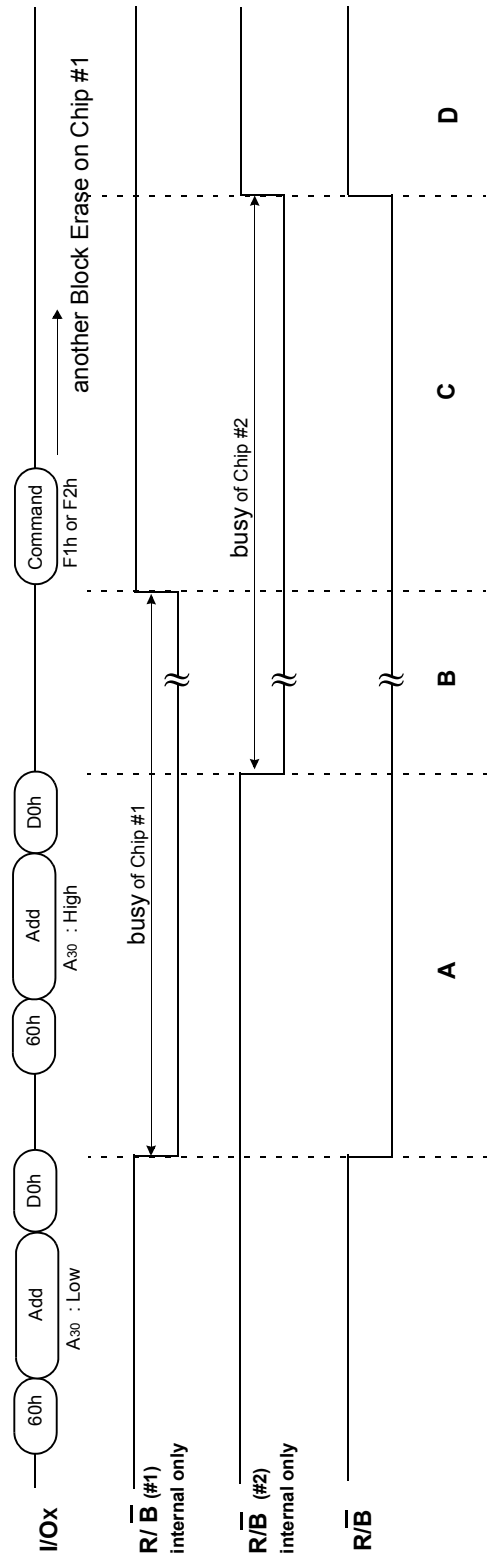
State C : Page program on chip #1 is terminated, but page program on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another page program command to chip #1.

State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate page program on chip #1 and chip #2 alternately.

| Status | Operation | Status Command / Data | |
|--------|--------------------------------|-----------------------|-----|
| | | F1h | F2h |
| A | Chip 1 : Busy, Chip 2 : Ready | 8xh | Cxh |
| B | Chip 1 : Busy, Chip 2 : Busy | 8xh | 8xh |
| C | Chip 1 : Ready, Chip 2 : Busy | Cxh | 8xh |
| D | Chip 1 : Ready, Chip 2 : Ready | Cxh | Cxh |

Interleave Block Erase



State A : Chip #1 is executing a block erase operation, and chip #2 is in ready state. So the host can issue a block erase command to chip #2.

State B : Both chip #1 and chip #2 are executing block erase operation.

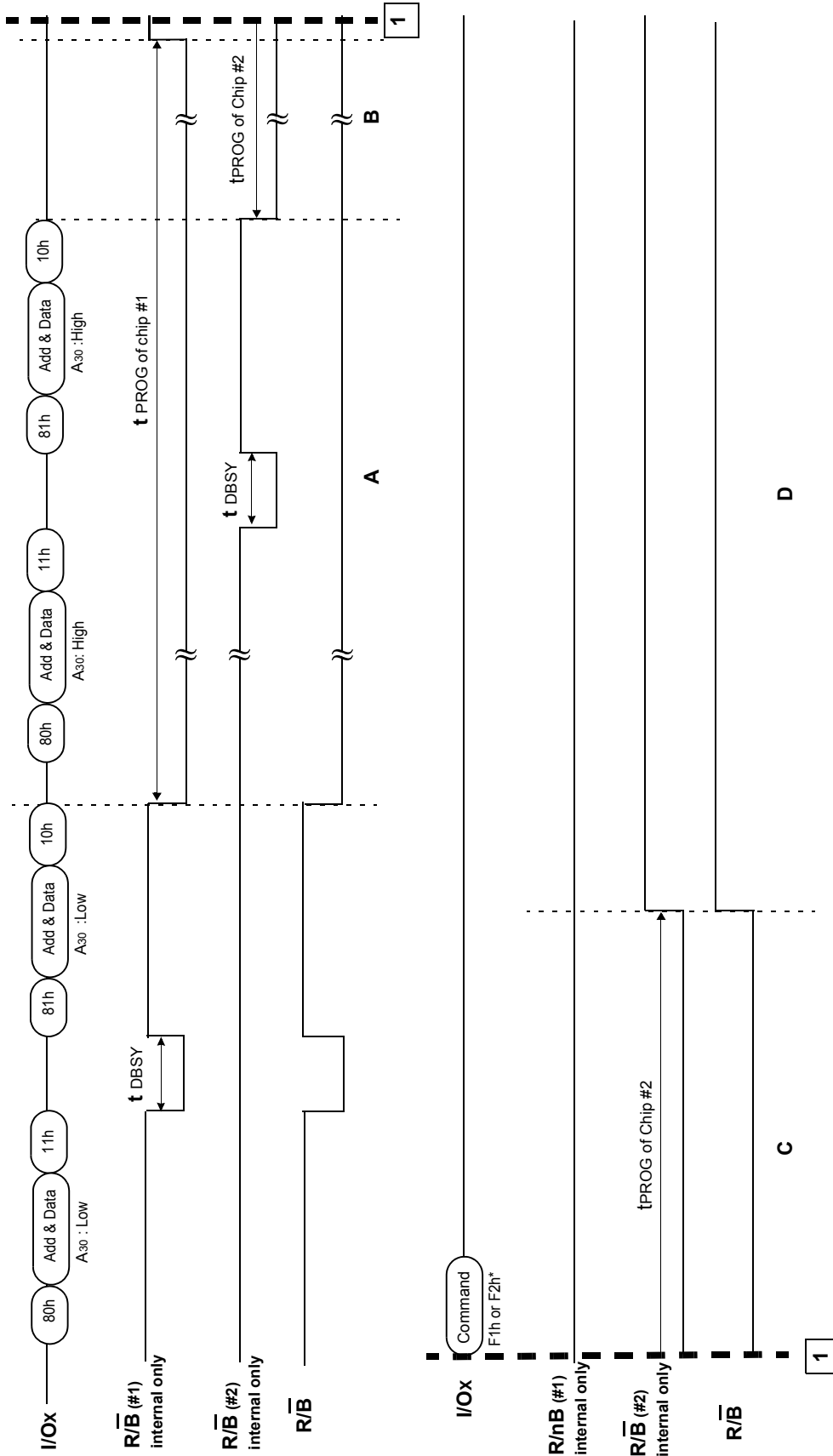
State C : Block erase on chip #1 is terminated, but block erase on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another block erase command to chip #1.

State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate block erase on chip #1 and chip #2 alternately.

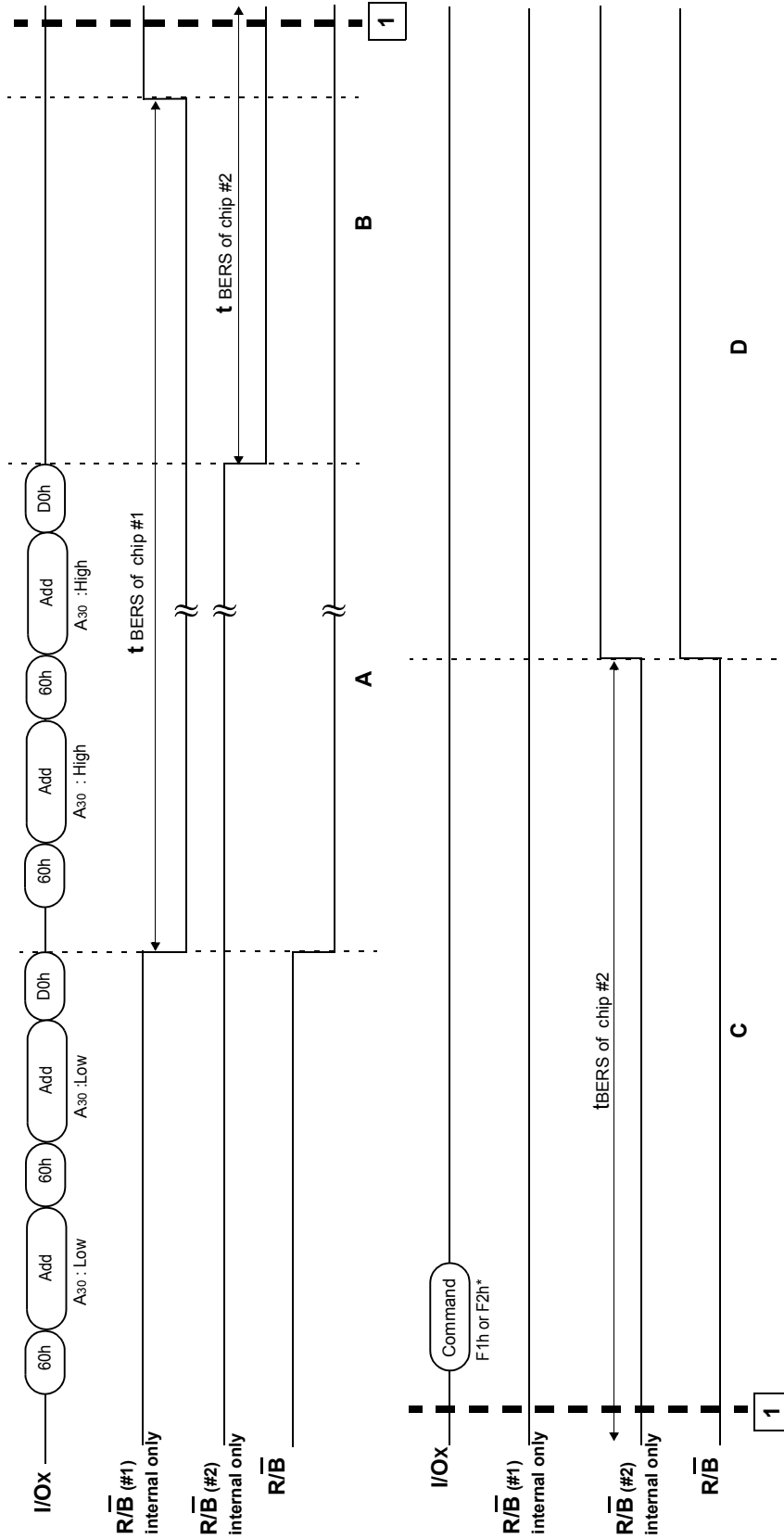
| Status | Operation | Status Command / Data | |
|--------|--------------------------------|-----------------------|-----|
| | | F1h | F2h |
| A | Chip 1 : Busy, Chip 2 : Ready | 8xh | Cxh |
| B | Chip 1 : Busy, Chip 2 : Busy | 8xh | 8xh |
| C | Chip 1 : Ready, Chip 2 : Busy | Cxh | 8xh |
| D | Chip 1 : Ready, Chip 2 : Ready | Cxh | Cxh |

Interleave Two-Plane Page Program



State A : Chip #1 is executing a page program operation, and chip #2 is in ready state. So the host can issue a page program command to chip #2.
State B : Both chip #1 and chip #2 are executing page program operation.
State C : Page program on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing page program operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next page program command to chip #1.
 F2h command is required to check the status of chip #2 to issue the next page program command to chip #2.
 According to the above process, the system can operate two-plane page program on chip #1 and chip #2 alternately.

Interleave Two-Plane Block Erase



State A : Chip #1 is executing a block erase operation, and chip #2 is in ready state. So the host can issue a block erase command to chip #2.

State B : Both chip #1 and chip #2 are executing block erase operation.

State C : Block erase on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing block erase operation.

State D : Both chip #1 and chip #2 are ready.

Note : *F1h command is required to check the status of chip #1 to issue the next block erase command to chip #1.

F2h command is required to check the status of chip #2 to issue the next block erase command to chip #2.

As the above process, the system can operate two-plane block erase on chip #1 and chip #2 alternatively.

System Interface Using $\overline{\text{CE}}$ don't-care.

For an easier system interface, $\overline{\text{CE}}$ may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ -seconds, de-activating $\overline{\text{CE}}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{\text{CE}}$ don't-care.

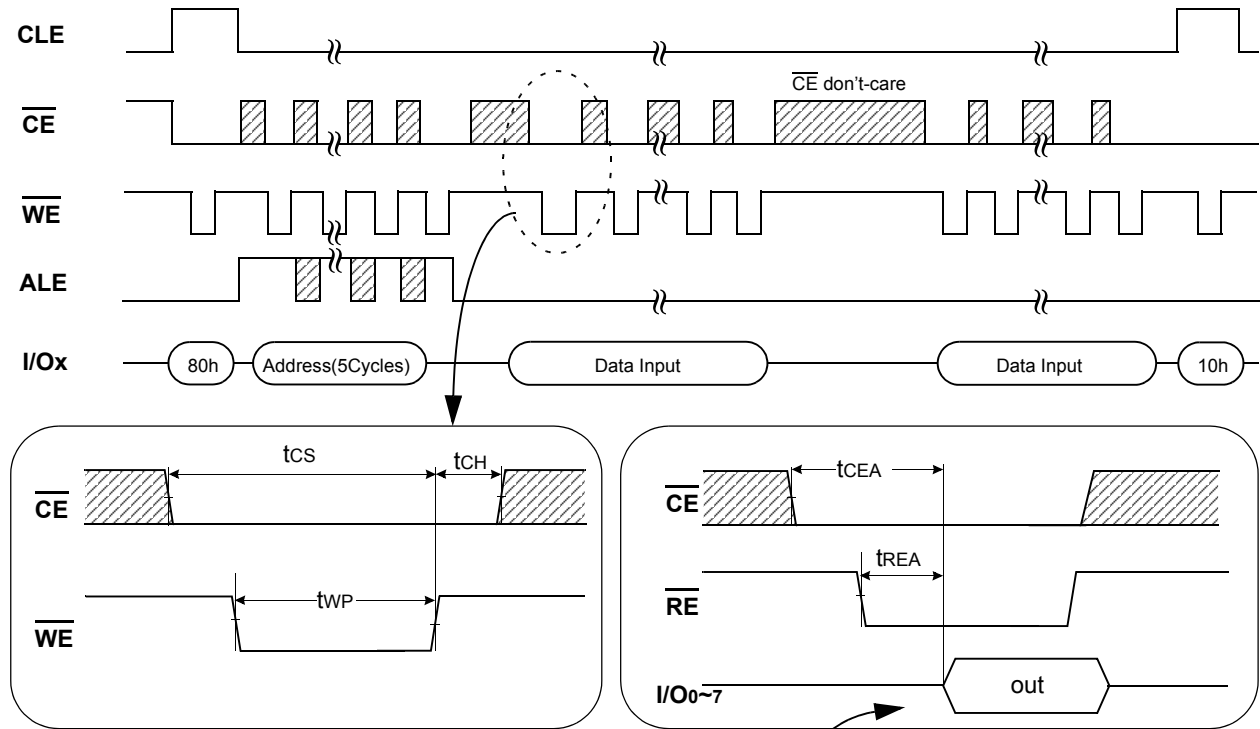
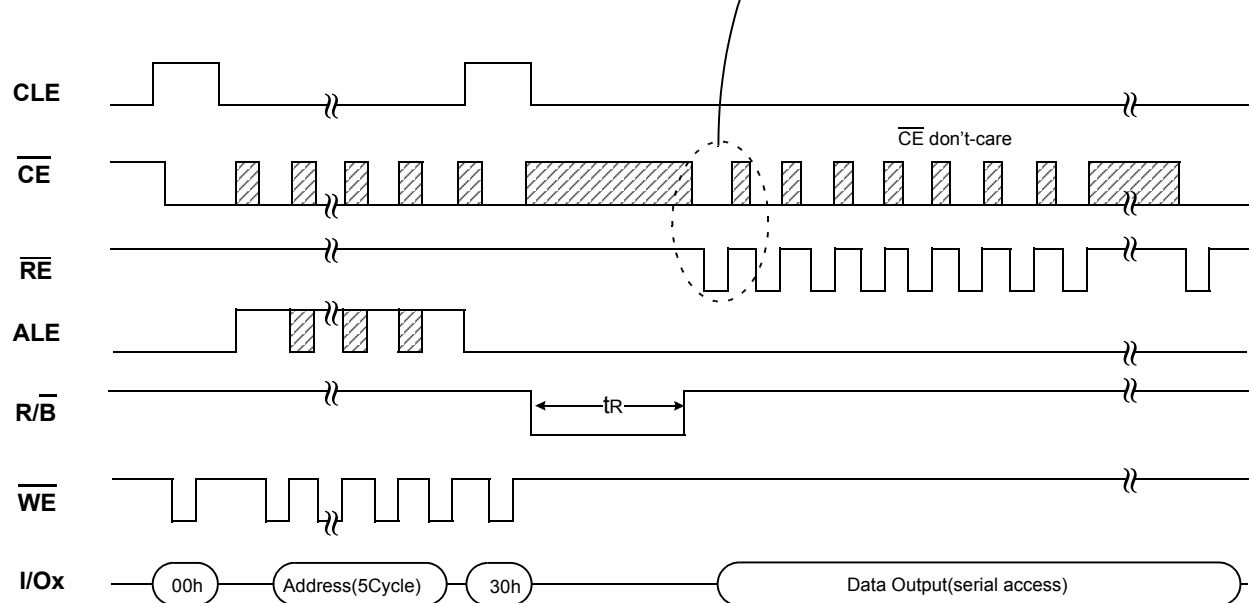


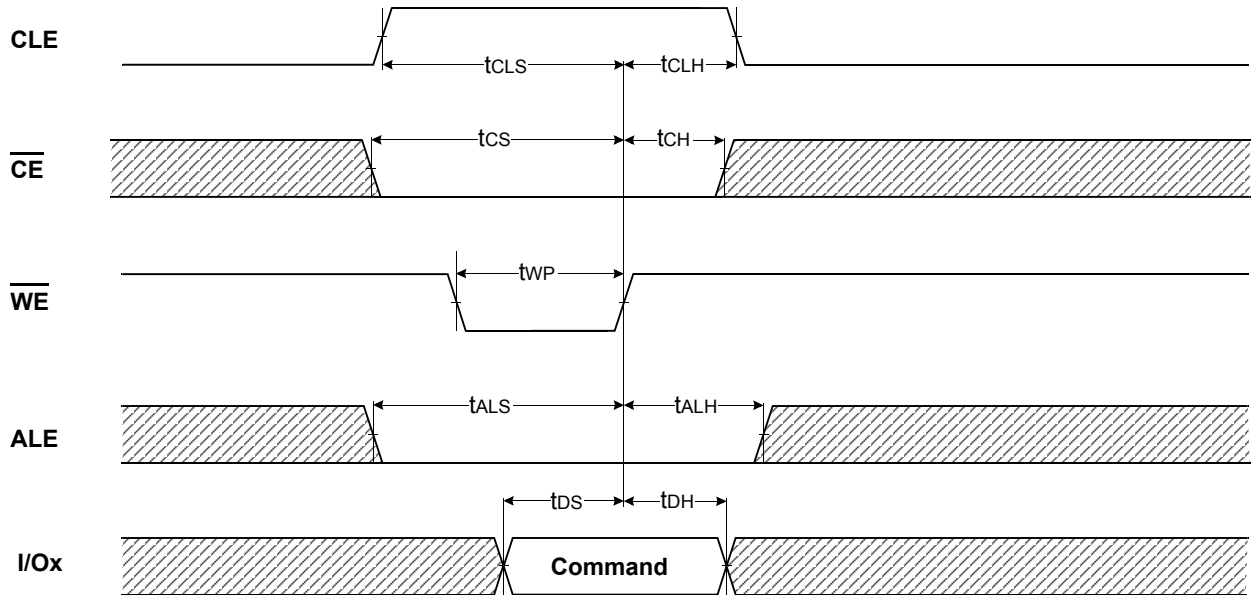
Figure 5. Read Operation with $\overline{\text{CE}}$ don't-care.



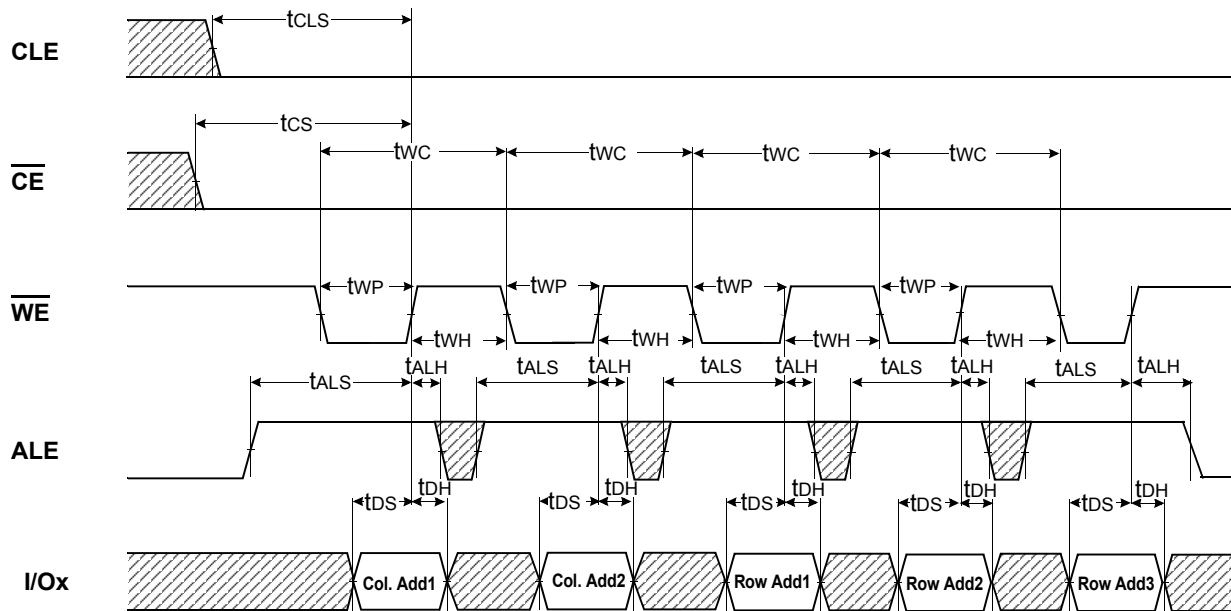
NOTE

| Device | I/O | DATA | ADDRESS | | | | |
|------------|---------------|-------------|-----------|-----------|----------|----------|----------|
| | I/Ox | Data In/Out | Col. Add1 | Col. Add2 | Row Add1 | Row Add2 | Row Add3 |
| K9K8G08U0A | I/O 0 ~ I/O 7 | 2,112byte | A0~A7 | A8~A11 | A12~A19 | A20~A27 | A28~A30 |

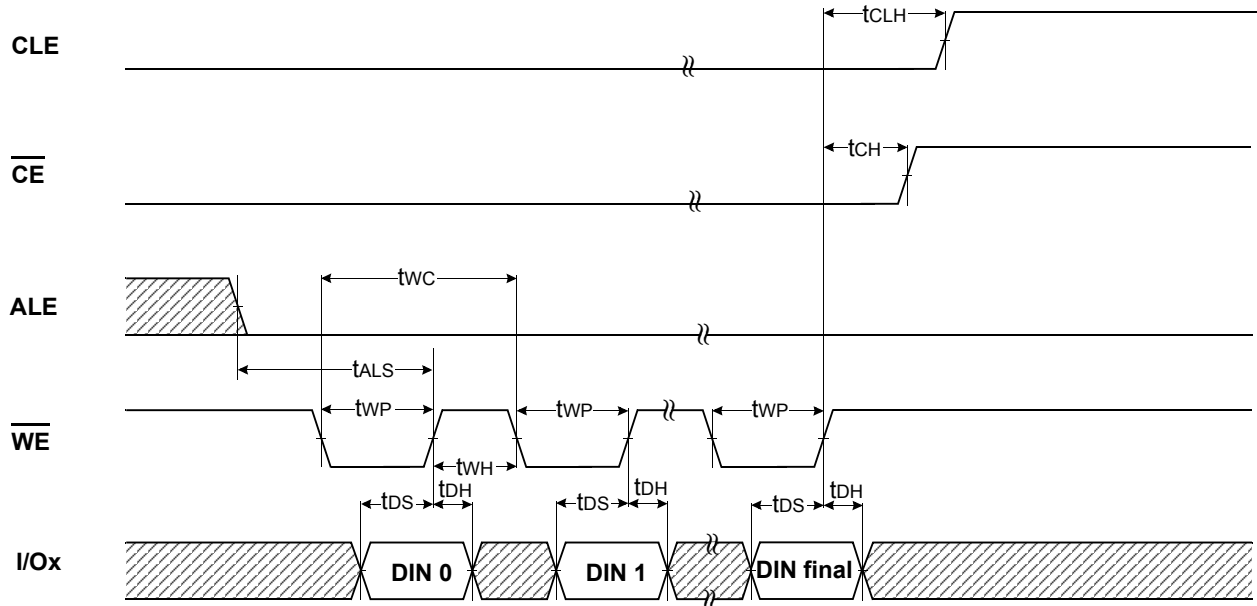
Command Latch Cycle



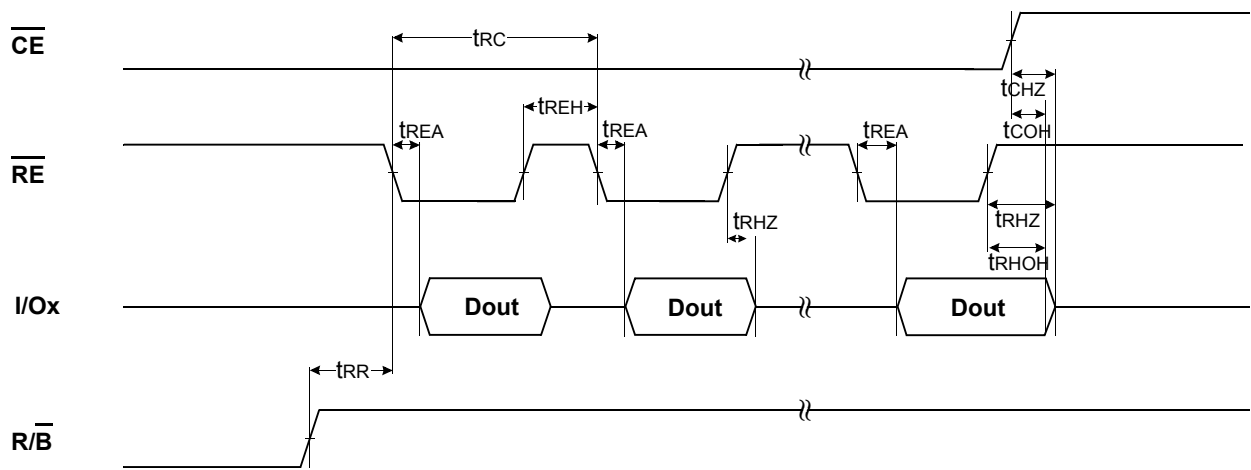
Address Latch Cycle



Input Data Latch Cycle

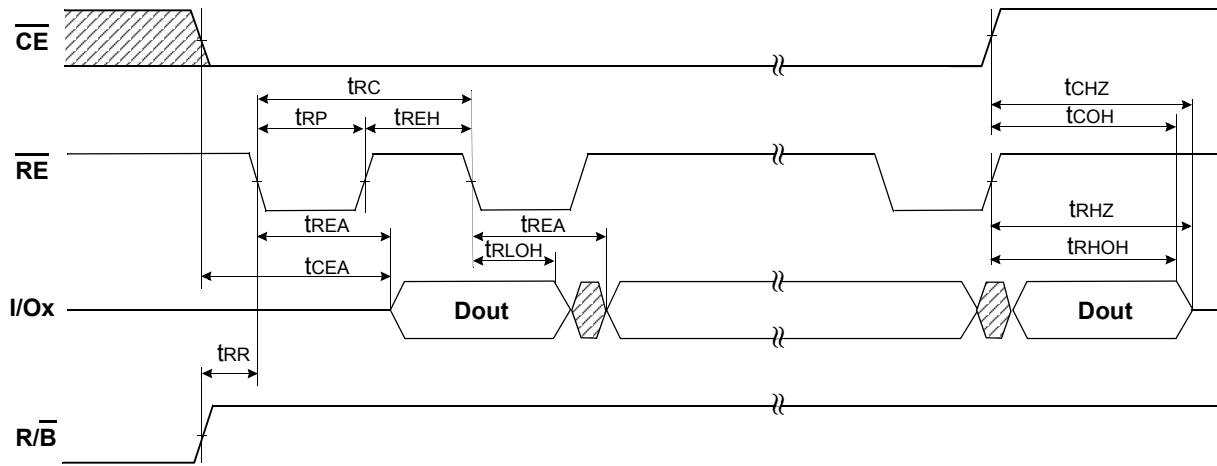


* Serial access Cycle after Read (CLE=L, WE=H, ALE=L)



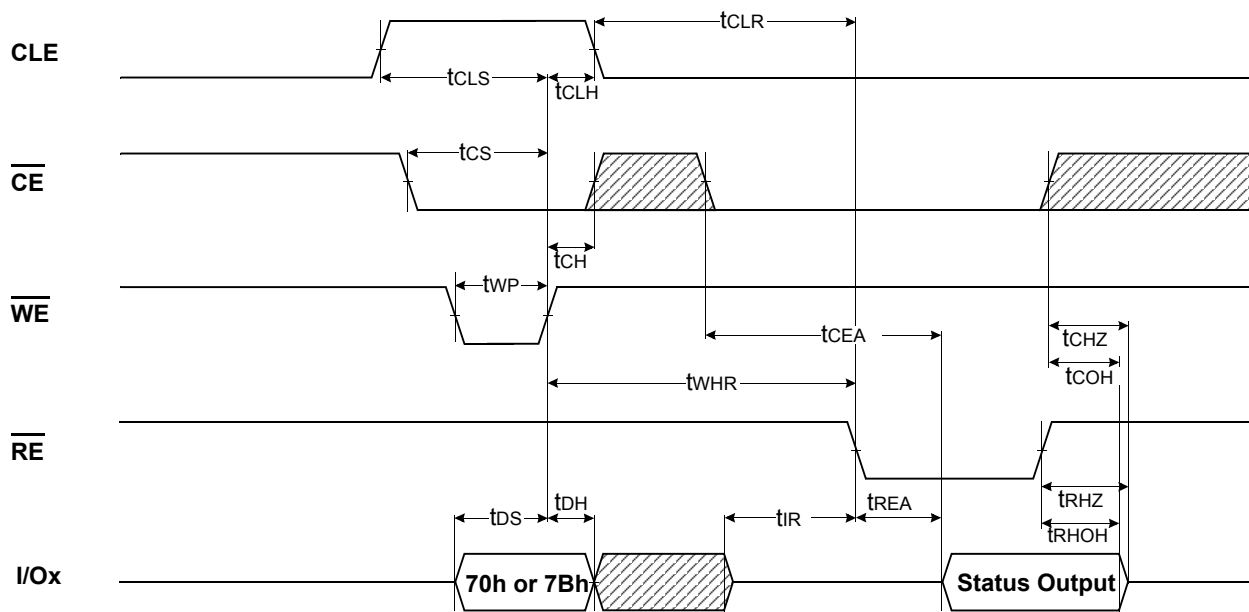
NOTES : Transition is measured at $\pm 200\text{mV}$ from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Serial Access Cycle after Read (EDO Type, CLE=L, \overline{WE} =H, ALE=L)

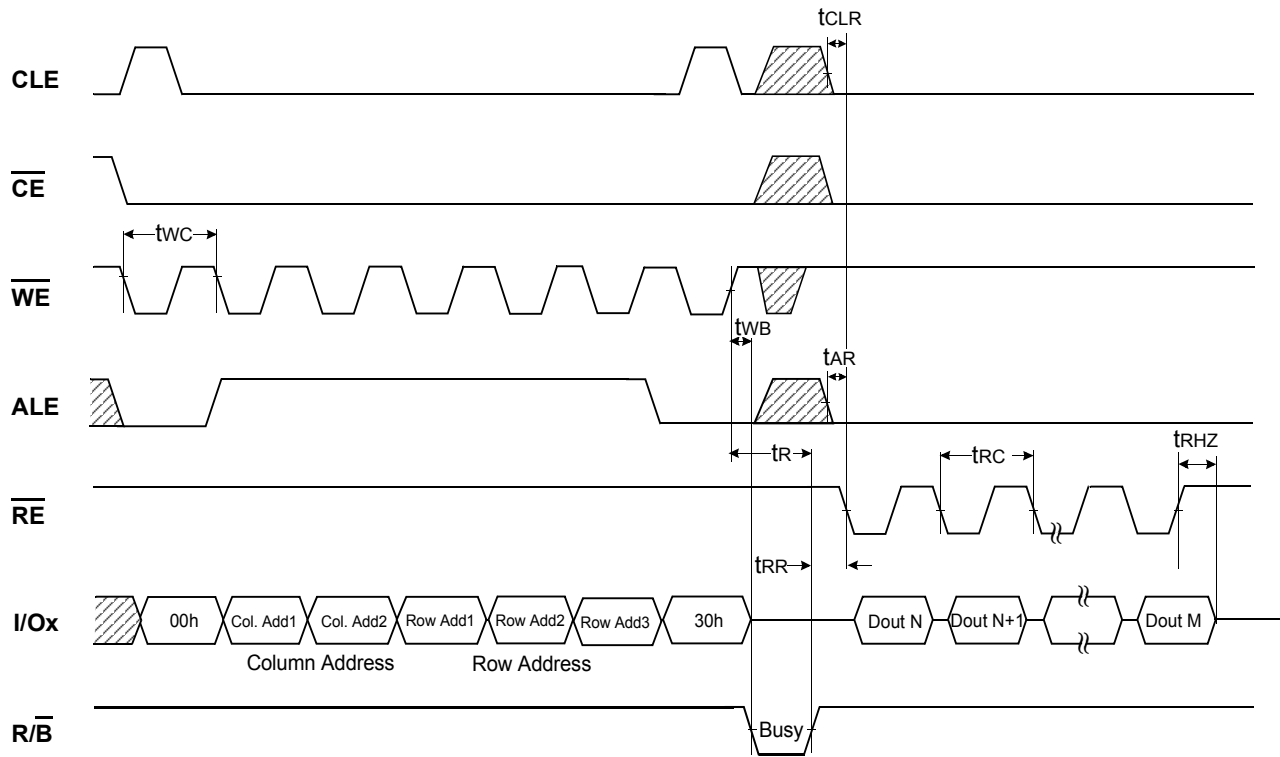


NOTES : Transition is measured at $\pm 200\text{mV}$ from steady state voltage with load.
This parameter is sampled and not 100% tested.
 t_{RLOH} is valid when frequency is higher than 33MHz.
 t_{RHOH} starts to be valid when frequency is lower than 33MHz.

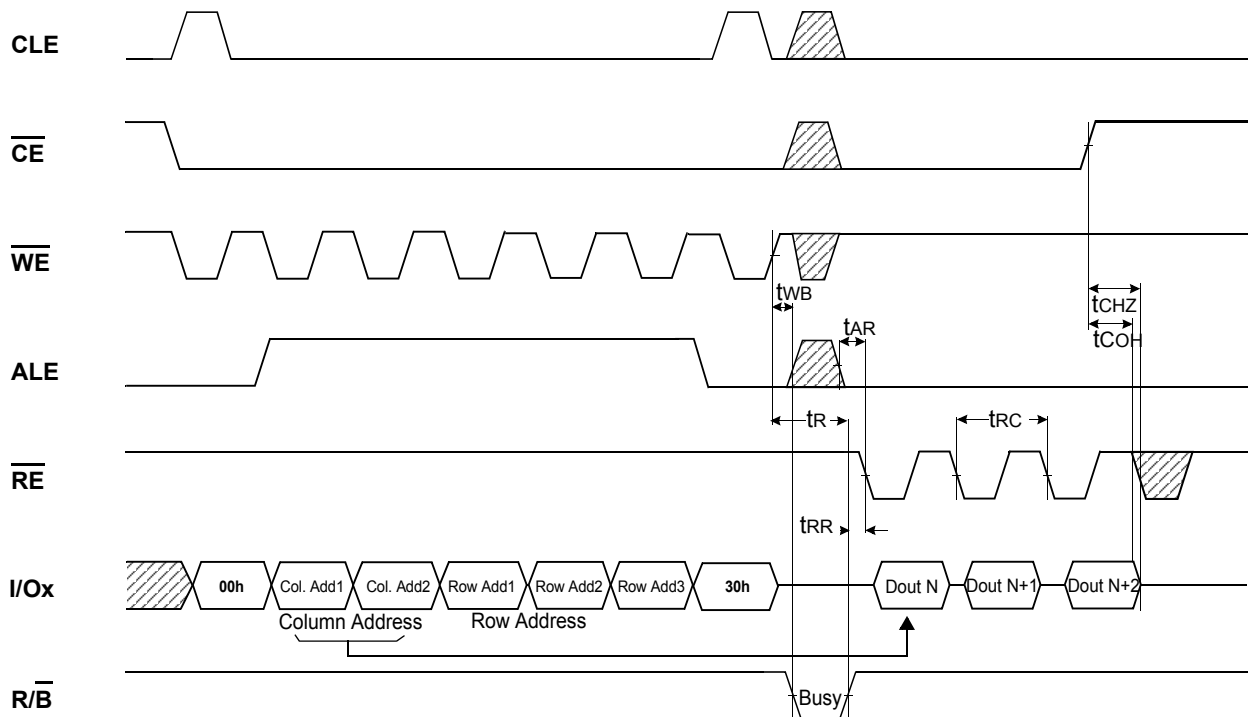
Status Read Cycle & EDC Status Read Cycle



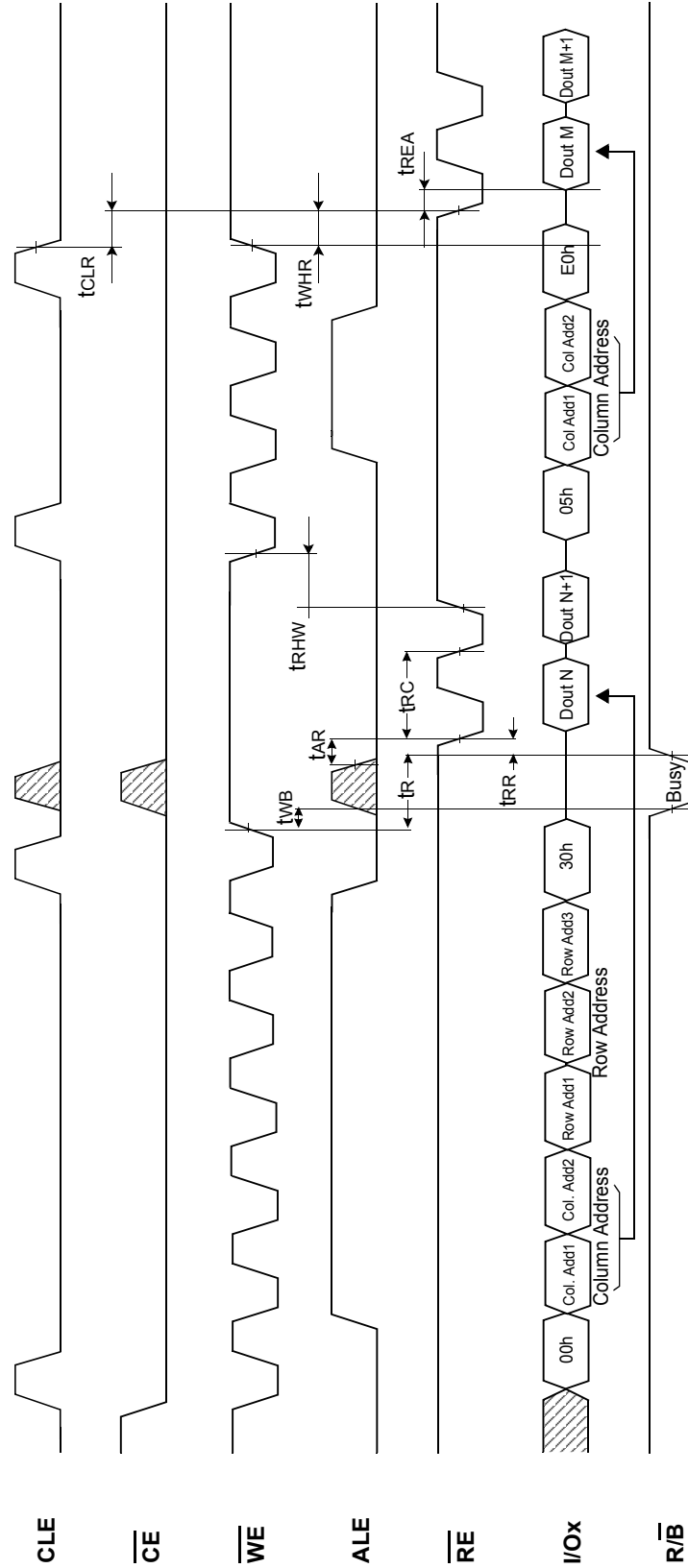
Read Operation



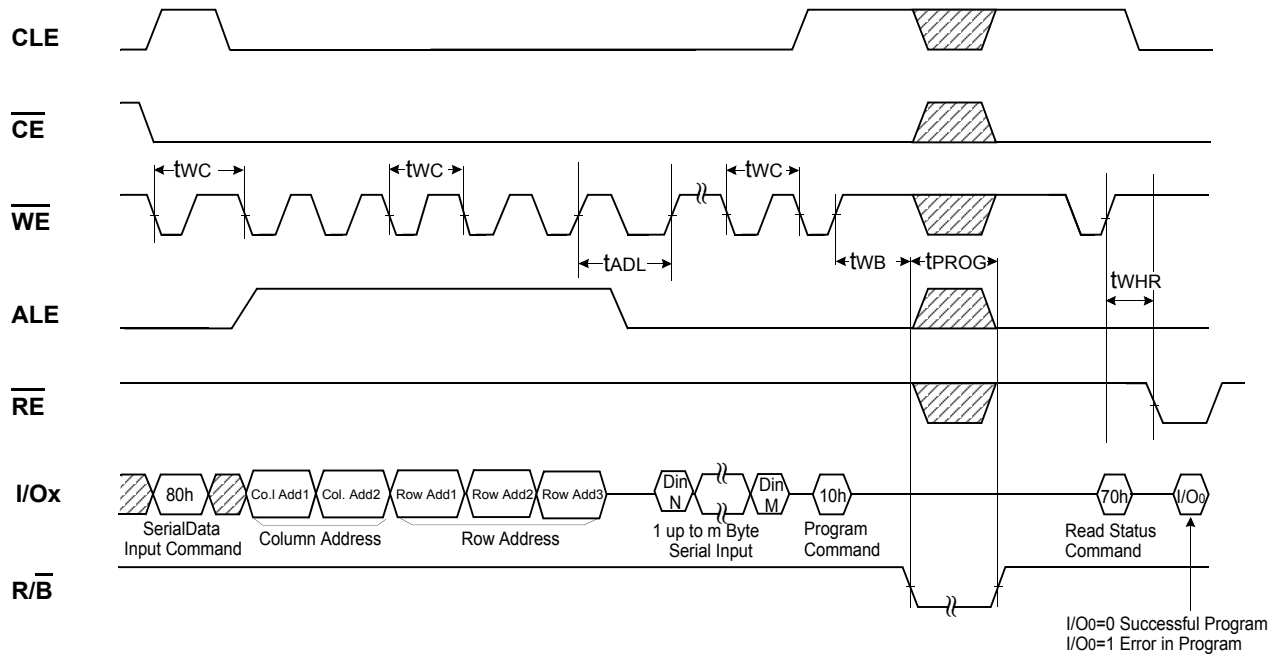
Read Operation (Intercepted by \overline{CE})



Random Data Output In a Page

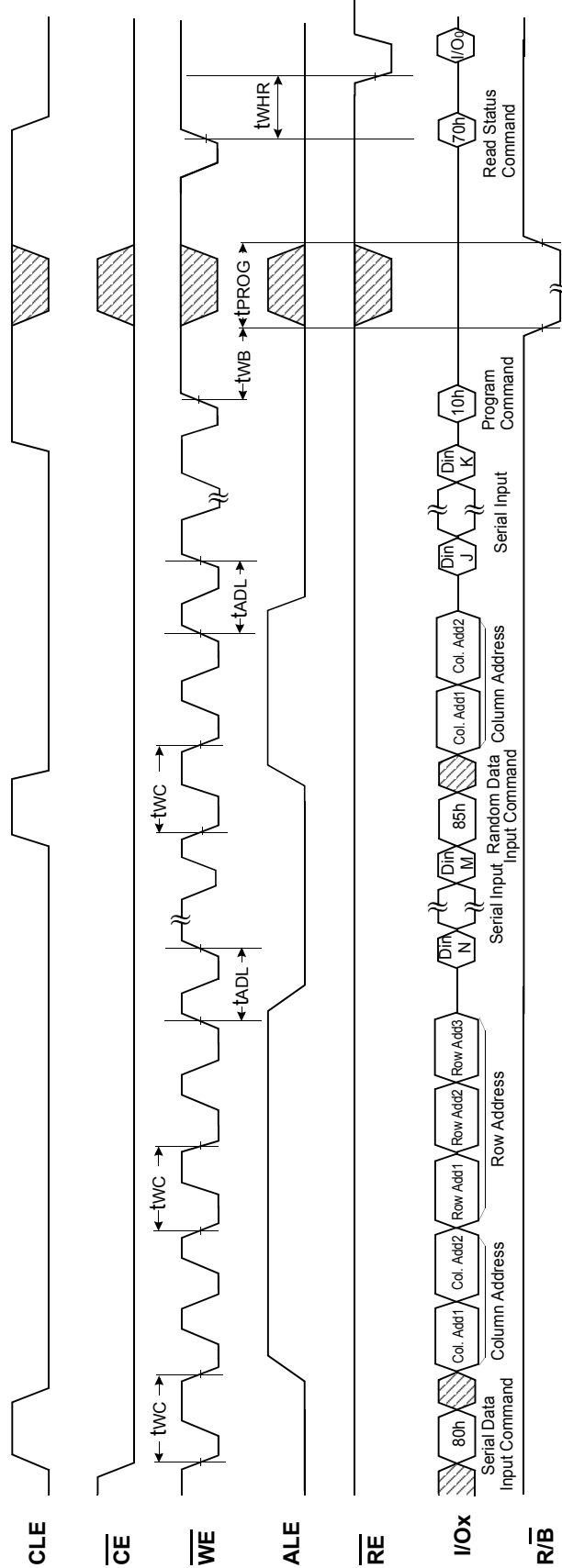


Page Program Operation



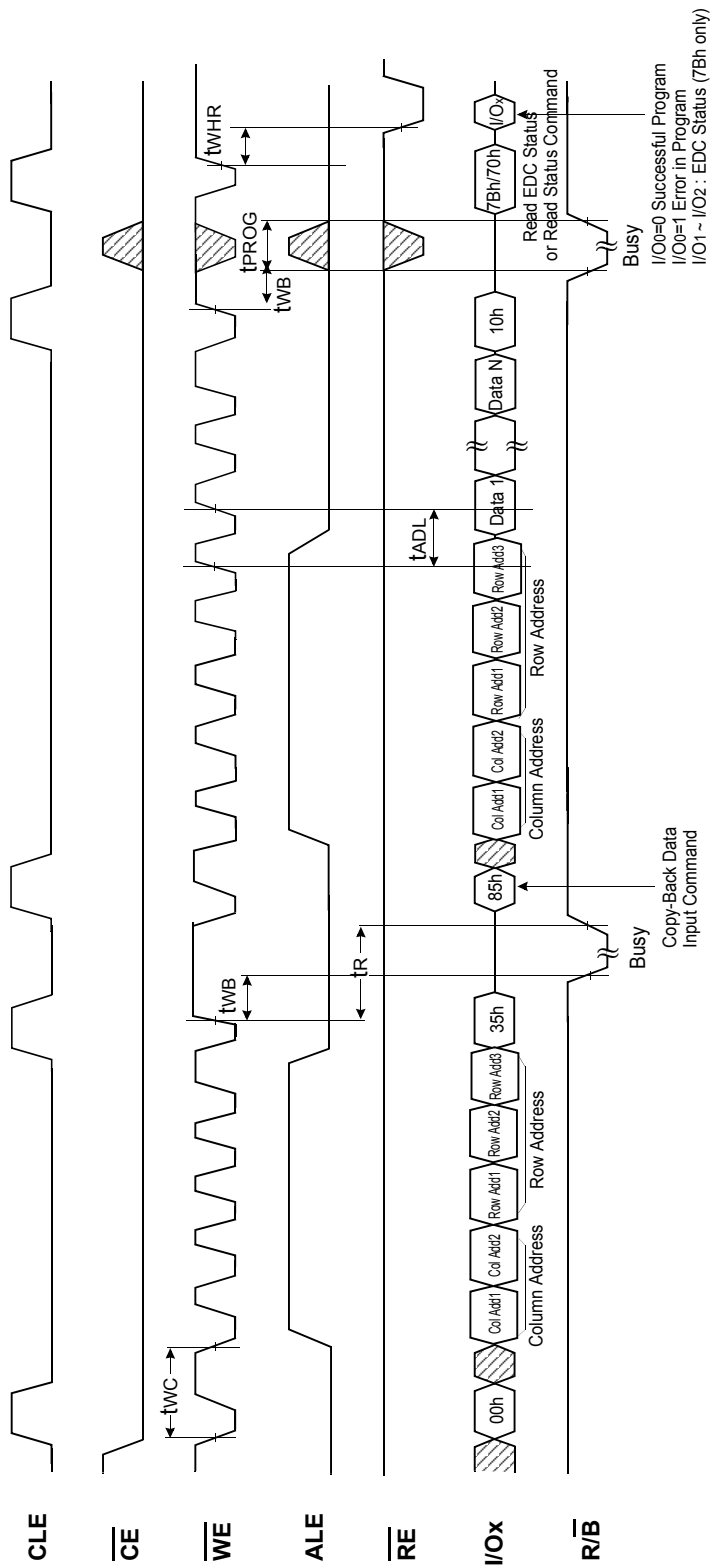
NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Page Program Operation with Random Data Input



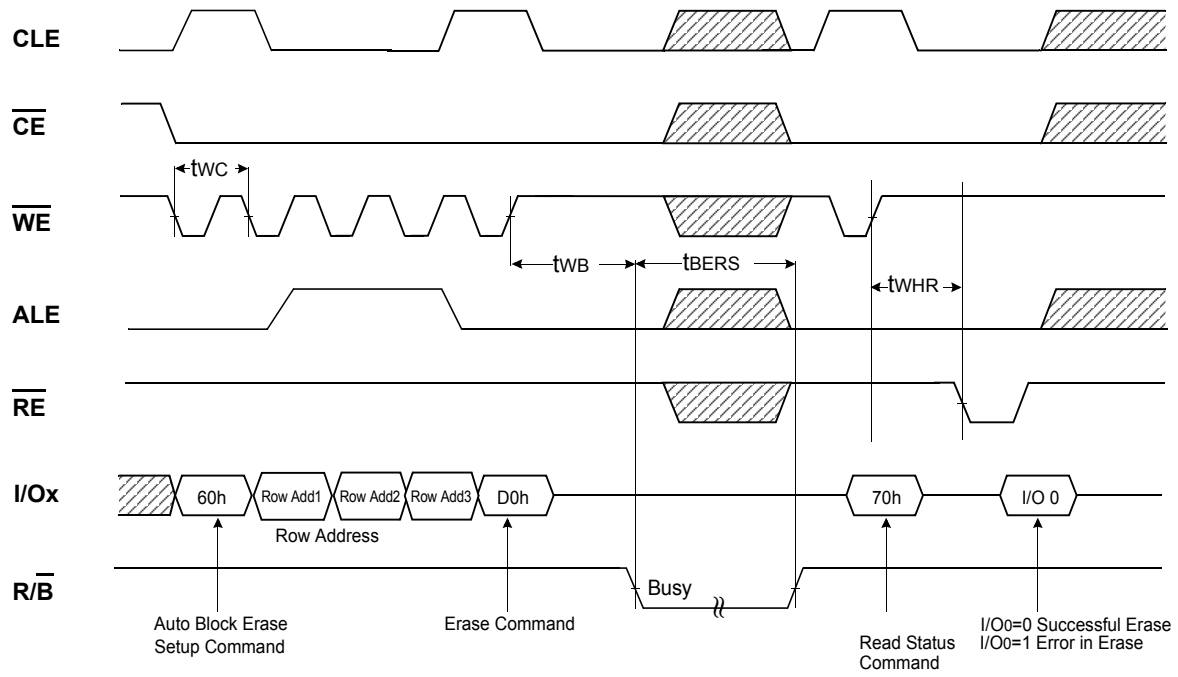
- NOTES :**
1. tADL is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.
 2. For EDC operation, only one time random data input is possible at the same address.

Copy-Back Program Operation With Random Data Input

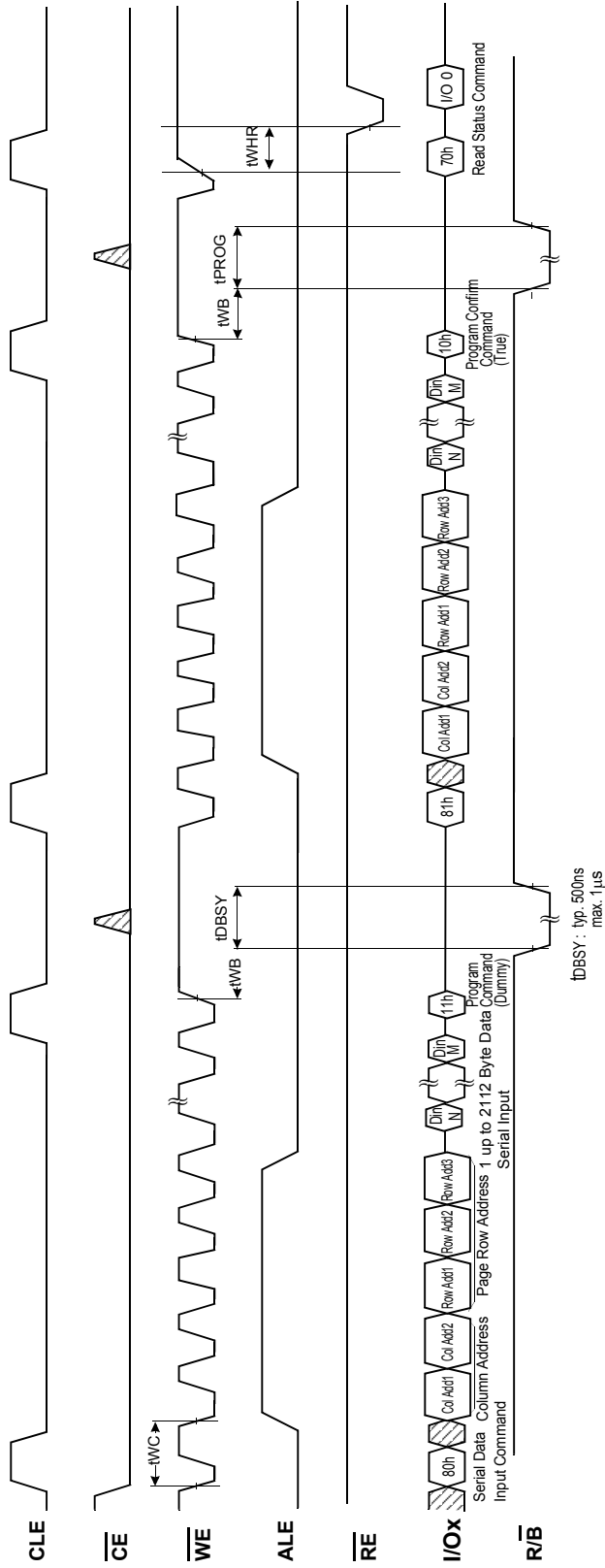


NOTES : 1. tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.
2. For EDC operation, only one time random data input is possible at the same address.

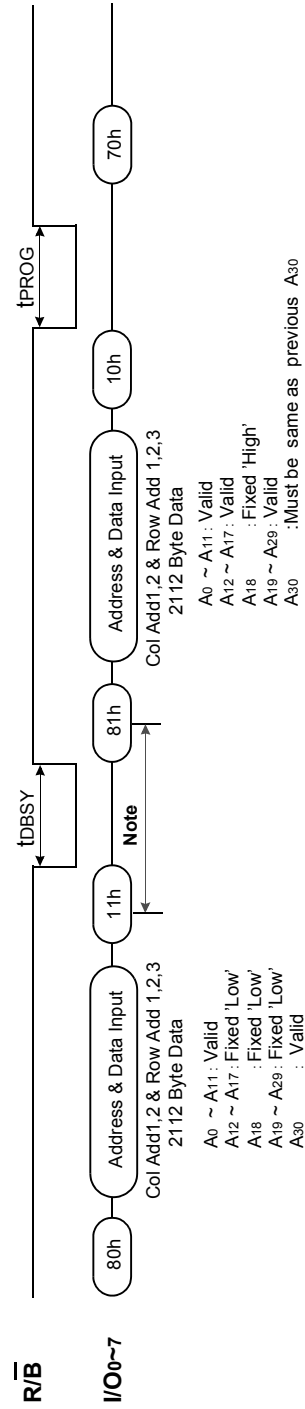
Block Erase Operation



Two-Plane Page Program Operation

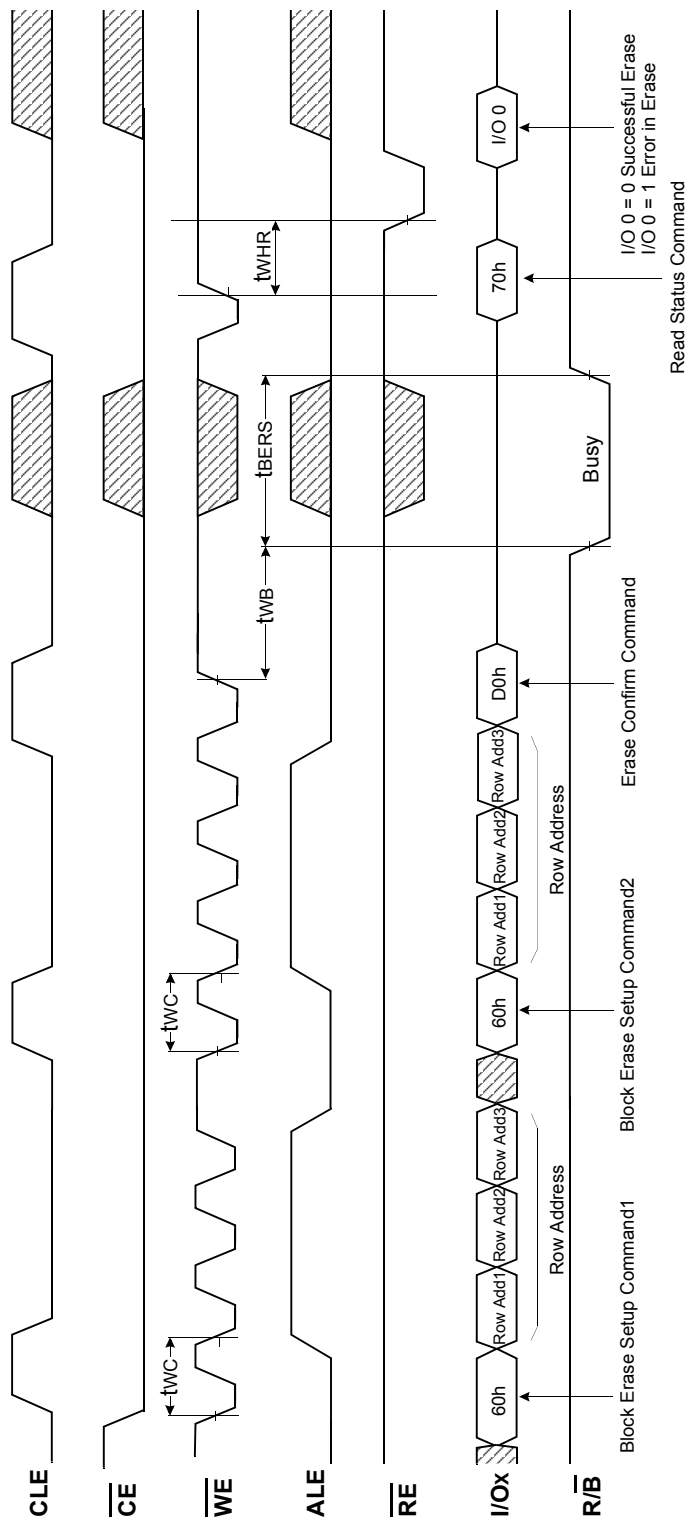


Ex.) Two-Plane Page Program



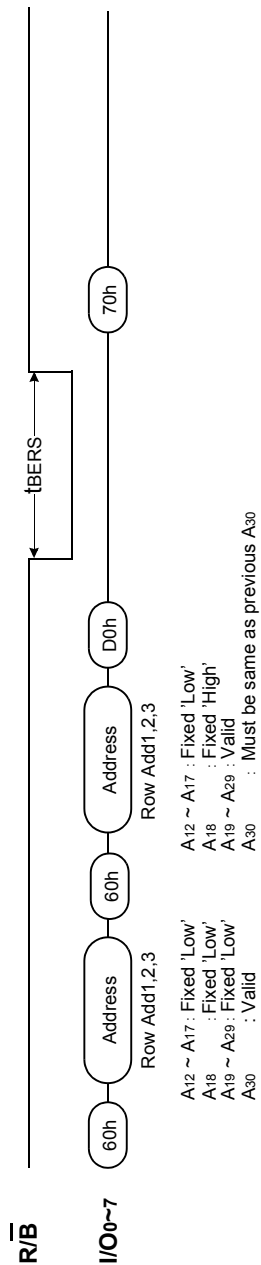
Note: Any command between 11h and 81h is prohibited except 70h and FFh.

Two-Plane Block Erase Operation

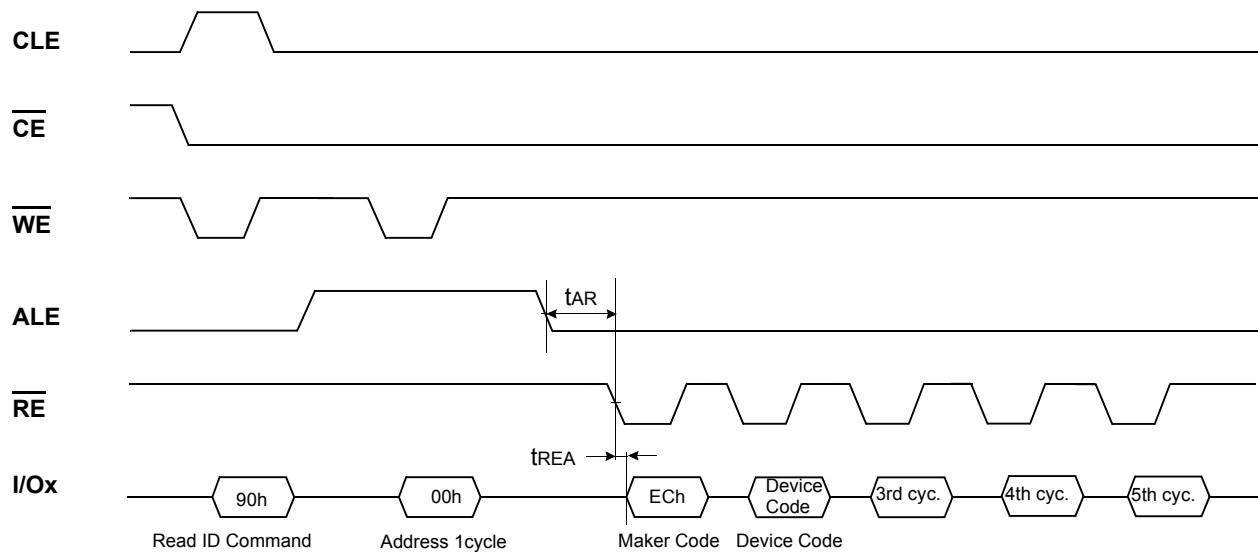


* For Two-Plane Erase operation, Block address to be erased should be repeated before "D0H" command.

Ex.) Address Restriction for Two-Plane Block Erase Operation



Read ID Operation



| Device | Device Code(2nd Cycle) | 3rd Cycle | 4th Cycle | 5th Cycle |
|------------|--------------------------|-----------|-----------|-----------|
| K9K8G08U0A | D3h | 51h | 95h | 58h |
| K9WAG08U1A | Same as K9K8G08U0A in it | | | |
| K9NBG08U5A | | | | |

ID Definition Table

90 ID : Access command = 90H

| | Description |
|----------------------|---|
| 1 st Byte | Maker Code |
| 2 nd Byte | Device Code |
| 3 rd Byte | Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc |
| 4 th Byte | Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum |
| 5 th Byte | Plane Number, Plane Size |

3rd ID Data

| | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---------------|------|------|------|------|------|------|------|------|
| Internal Chip Number | 1 | | | | | | | 0 | 0 |
| | 2 | | | | | | | 0 | 1 |
| | 4 | | | | | | | 1 | 0 |
| | 8 | | | | | | | 1 | 1 |
| Cell Type | 2 Level Cell | | | | | 0 | 0 | | |
| | 4 Level Cell | | | | | 0 | 1 | | |
| | 8 Level Cell | | | | | 1 | 0 | | |
| | 16 Level Cell | | | | | 1 | 1 | | |
| Number of Simultaneously Programmed Pages | 1 | | | 0 | 0 | | | | |
| | 2 | | | 0 | 1 | | | | |
| | 4 | | | 1 | 0 | | | | |
| | 8 | | | 1 | 1 | | | | |
| Interleave Program Between multiple chips | Not Support | | 0 | | | | | | |
| | Support | | 1 | | | | | | |
| Cache Program | Not Support | 0 | | | | | | | |
| | Support | 1 | | | | | | | |

4th ID Data

| | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|-------------------------------------|-------------|------|------|------|------|------|------|------|------|
| Page Size (w/o redundant area) | 1KB | | | | | | | 0 | 0 |
| | 2KB | | | | | | | 0 | 1 |
| | 4KB | | | | | | | 1 | 0 |
| | 8KB | | | | | | | 1 | 1 |
| Block Size (w/o redundant area) | 64KB | | | 0 | 0 | | | | |
| | 128KB | | | 0 | 1 | | | | |
| | 256KB | | | 1 | 0 | | | | |
| | 512KB | | | 1 | 1 | | | | |
| Redundant Area Size (byte/512byte) | 8 | | | | | | 0 | | |
| | 16 | | | | | | 1 | | |
| Organization | x8 | | 0 | | | | | | |
| | x16 | | 1 | | | | | | |
| Serial Access Minimum | 50ns/30ns | 0 | | | | 0 | | | |
| | 25ns | 1 | | | | 0 | | | |
| | Reserved | 0 | | | | 1 | | | |
| | Reserved | 1 | | | | 1 | | | |

5th ID Data

| | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|------------------------------------|-------------|------|------|------|------|------|------|------|------|
| Plane Number | 1 | | | | | 0 | 0 | | |
| | 2 | | | | | 0 | 1 | | |
| | 4 | | | | | 1 | 0 | | |
| | 8 | | | | | 1 | 1 | | |
| Plane Size (w/o redundant Area) | 64Mb | | 0 | 0 | 0 | | | | |
| | 128Mb | | 0 | 0 | 1 | | | | |
| | 256Mb | | 0 | 1 | 0 | | | | |
| | 512Mb | | 0 | 1 | 1 | | | | |
| | 1Gb | | 1 | 0 | 0 | | | | |
| | 2Gb | | 1 | 0 | 1 | | | | |
| | 4Gb | | 1 | 1 | 0 | | | | |
| 8Gb | | 1 | 1 | 1 | | | | | |
| Reserved | | 0 | | | | | | 0 | 0 |

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 20μs(t_R). The system controller can detect the completion of this data transfer(t_R) by analyzing the output of $\overline{R/B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns(K9NBG08U5A:50ns) cycle time by sequentially pulsing \overline{RE} . The repetitive high to low transitions of the \overline{RE} clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

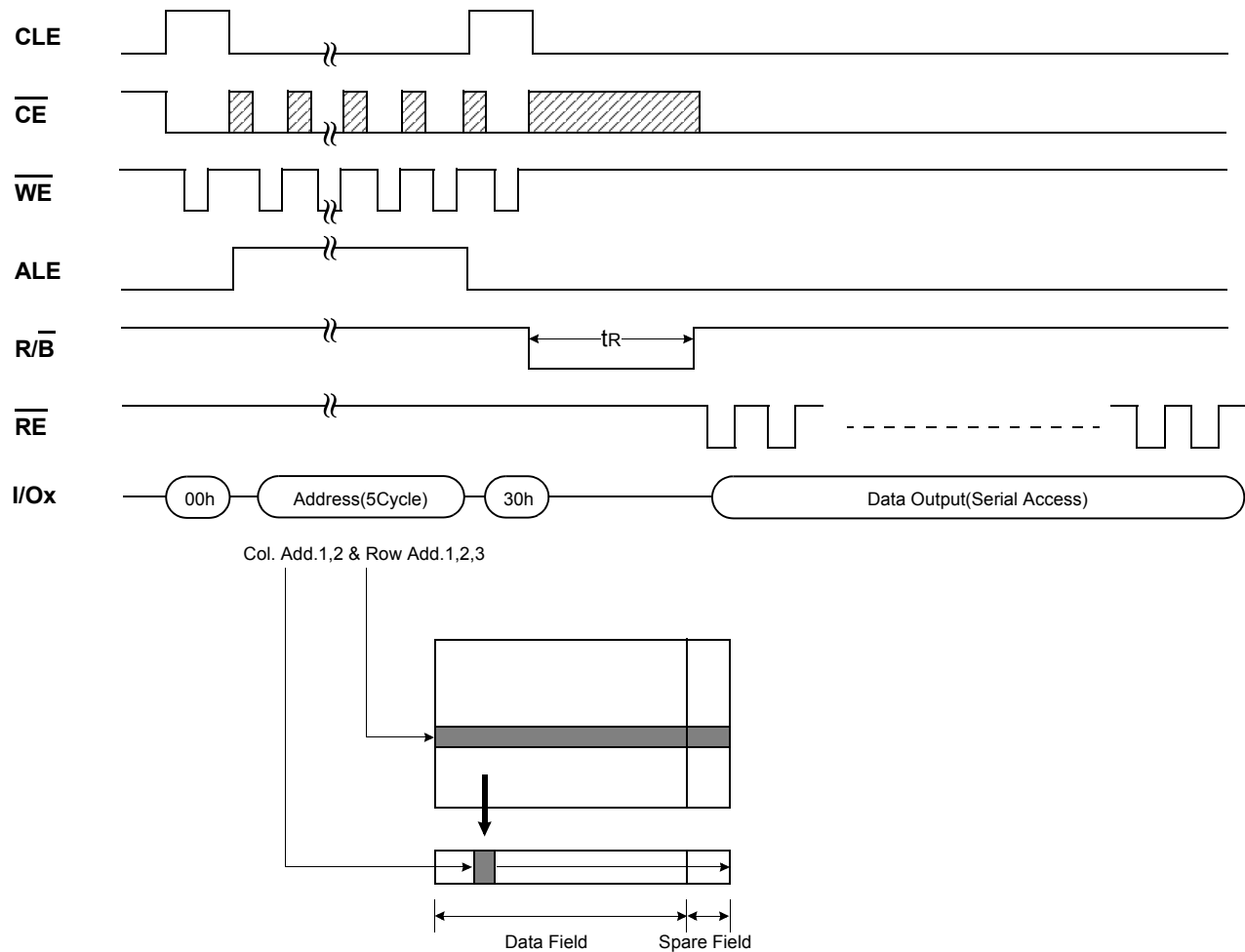
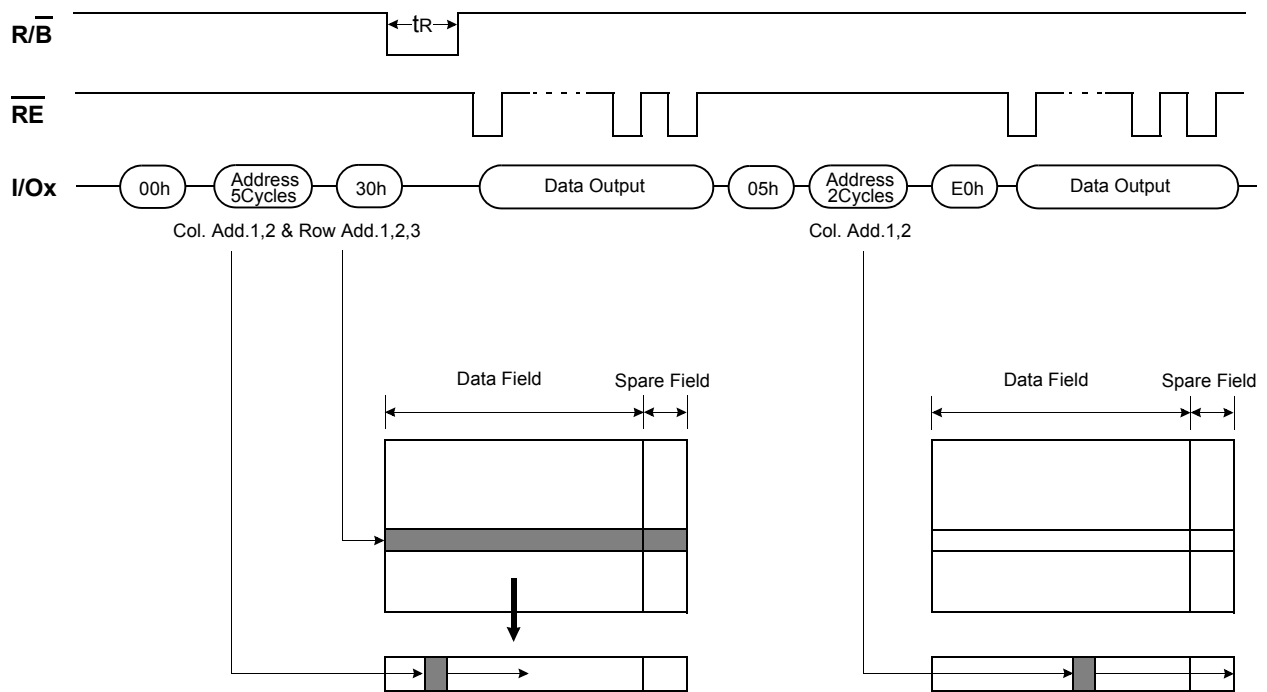


Figure 7. Random Data Output In a Page



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a word or consecutive bytes up to 2,112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for a single page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

Modifying the data of a sector by Random Data Input before Copy-Back Program must be performed for the whole sector and is allowed only once per each sector. Any partial modification smaller than a sector corrupts the on-chip EDC codes.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

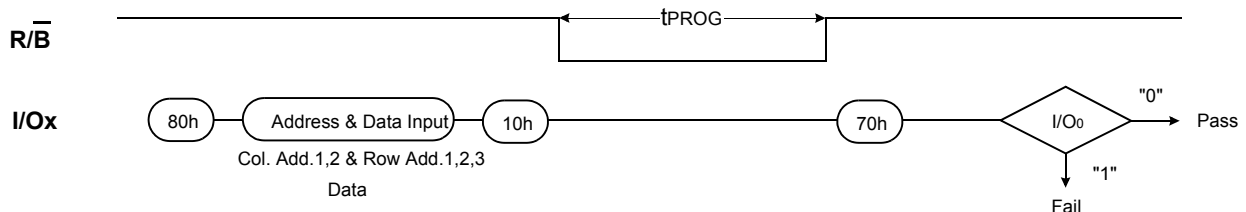
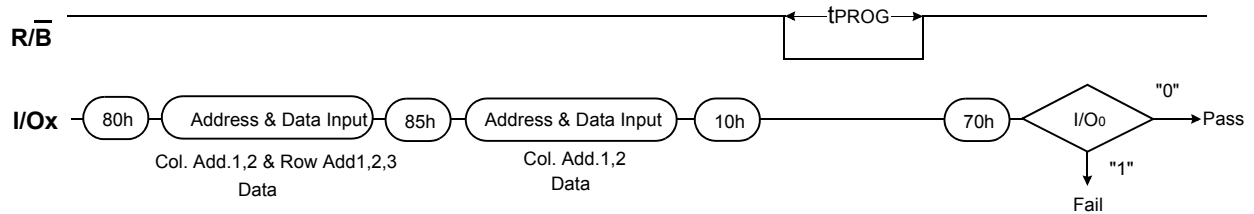


Figure 9. Random Data Input In a Page



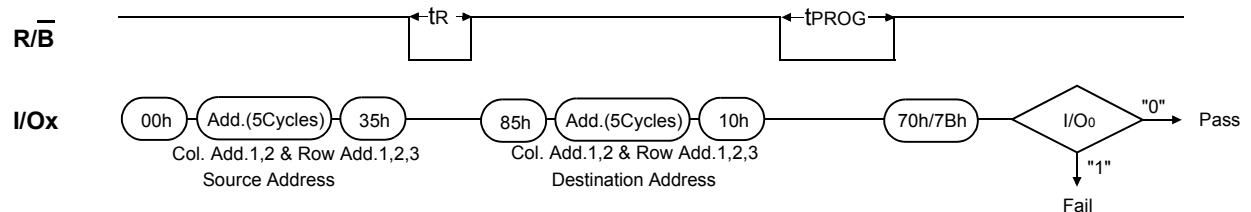
Copy-Back Program

The Copy-Back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. During tPROG, the device executes EDC of itself. Once the program process starts, the Read Status Register command (70h) or Read EDC Status command (7Bh) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) and EDC Status Bits (I/O 1 ~ I/O 2) may be checked(Figure 10 & Figure 11& Figure 12). The internal write verification detects only errors for "1"s that are not successfully programmed to "0"s and the internal EDC checks whether there is only 1-bit error for each 528-byte sector of the source page. More than 2-bit error detection is not available for each 528-byte sector. The command register remains in Read Status command mode or Read EDC Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h) as shown in Figure11. But EDC status Bits are not available during copy back for some bits or bytes modified by Random Data Input operation.

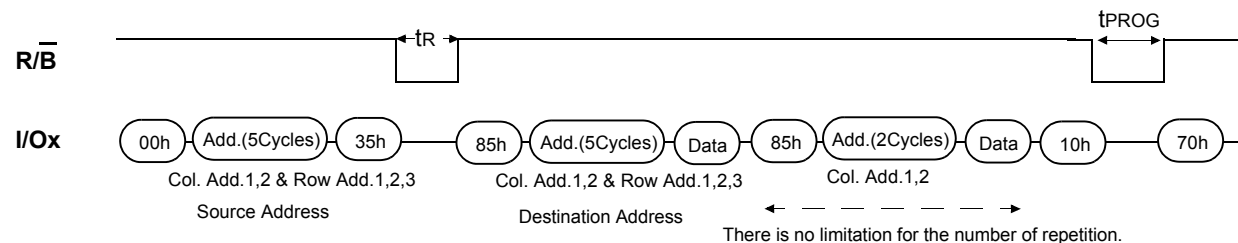
However, in case of the 528 byte sector unit modification, EDC status bits are available.

Figure 10. Page Copy-Back Program Operation



- Note:** 1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.

Figure 11. Page Copy-Back Program Operation with Random Data Input

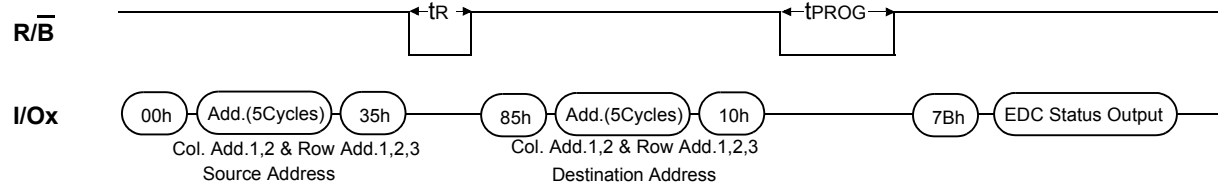


- Note:** 1. For EDC operation, only one time random data input is possible at the same address.

EDC OPERATION

Note that for the user who use Copy-Back with EDC mode, only one time random data input is possible at the same address during Copy-Back program or page program mode. For the user who use Copy-Back without EDC, there is no limitation for the random data input at the same address.

Figure 12. Page Copy-Back Program Operation with EDC & Read EDC Status

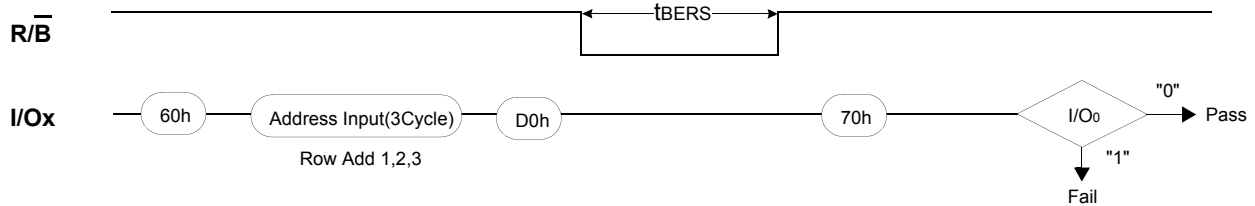


BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{30} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of \overline{WE} after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation

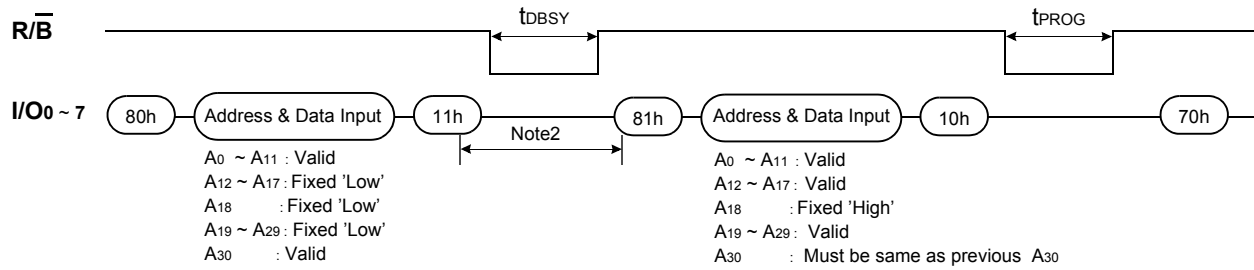


Two-Plane Page Program

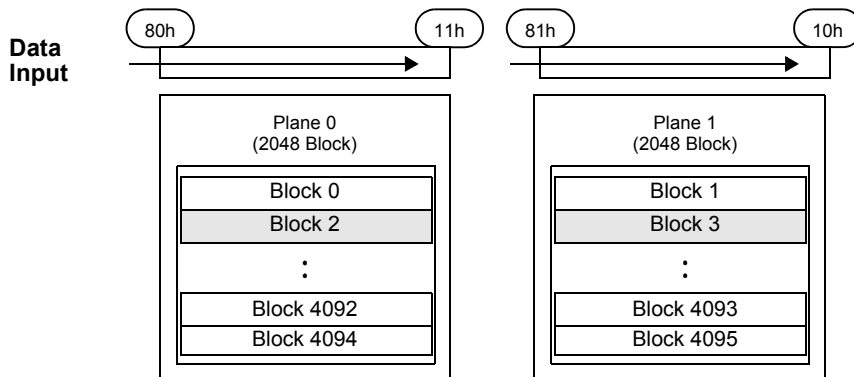
Two-Plane Page Program is an extension of Page Program, for a single plane with 2112 byte page registers. Since the device is equipped with four memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages. But there is some restriction, two-plane program operations can be executed by dividing the memory array into plane 0~1 or plane 2~3 separately. For example, two-plane program operation into plane 0 and plane 2 is prohibited. That is to say, two-plane program operation into plane 0 and plane 1 or into plane 2 and plane 3 is allowed.

After writing the first set of data up to 2112 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, $\overline{R/B}$ remains in Busy state for a short period of time(t_{DBSY}). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of $\overline{R/B}$ and Read Status is the same as that of Page Program. Although two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails. Restriction in addressing with Two-Plane Page Program is shown is Figure14.

Figure 14. Two-Plane Page Program



NOTE : 1. It is noticeable that same row address except for A₁₈ is applied to the two blocks
 2. Any command between 11h and 81h is prohibited except 70h and FFh.



NOTE : It is an example for two-plane page program into plane 0~1 (In this case, A₃₀ is low), and the method for two-plane page program into plane 2~3 is same. two-plane page program into plane 0&2 (or plane 0&3, or plane 1&2, or plane 1&3) is prohibited.

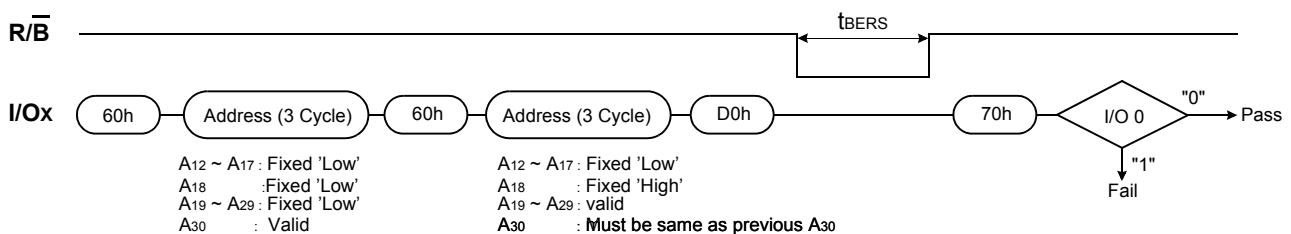
Two-Plane Block Erase

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/B pin or Ready/Busy status bit (I/O 6).

Two-plane erase operations can be executed by dividing the memory array into plane 0~1 or plane 2~3 separately.

For example, two-plane erase operation into plane 0 and plane 2 is prohibited. That is to say, two-plane erase operation into plane 0 and plane 1 or into plane 2 and plane 3 is allowed.

Figure 15. Two-Plane Block Erase Operation

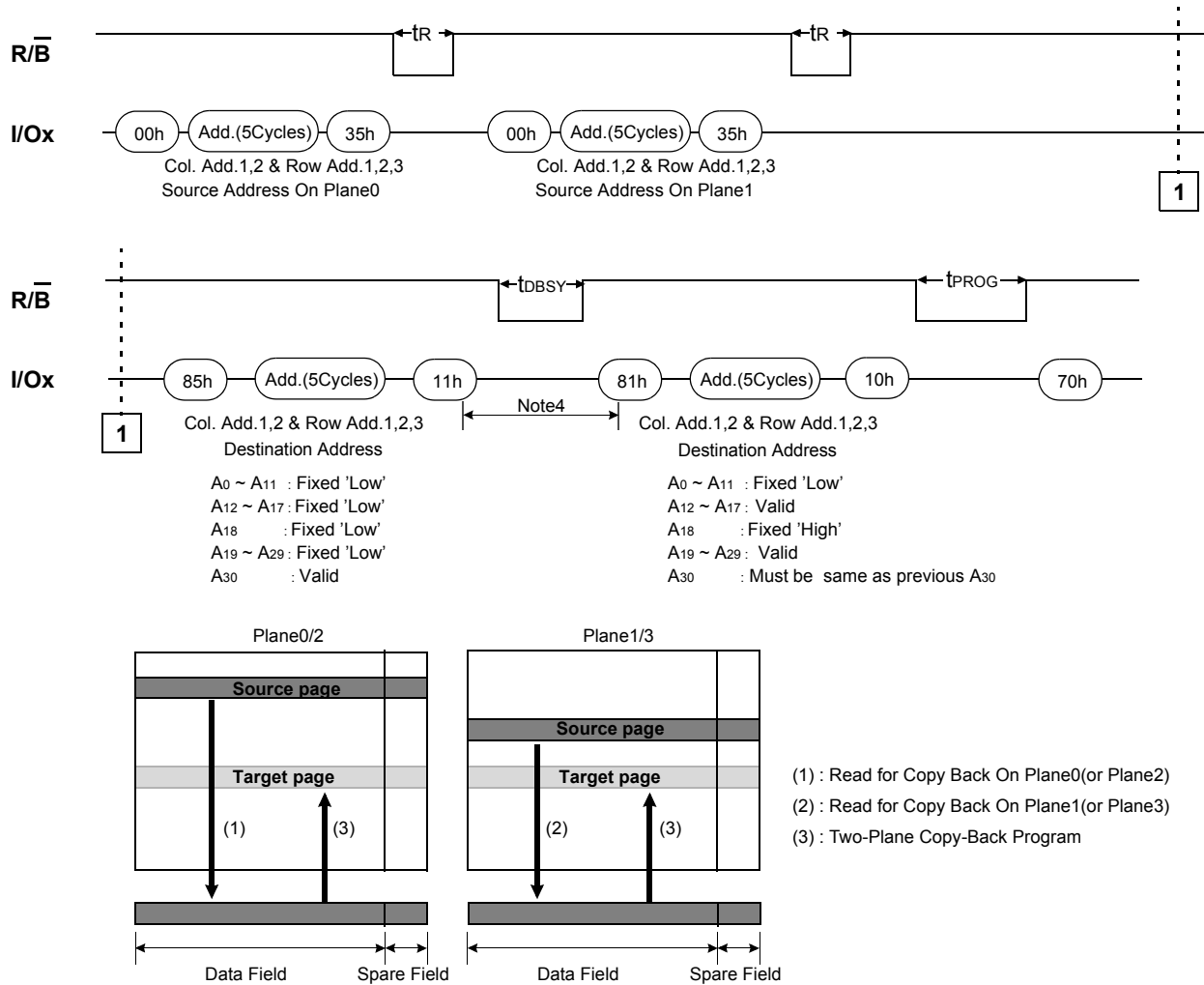


NOTE : Two-plane block erase into plane 0&2 (or plane 0&3, or plane 1&2, or plane 1&3) is prohibited.

Two-Plane Copy-Back Program

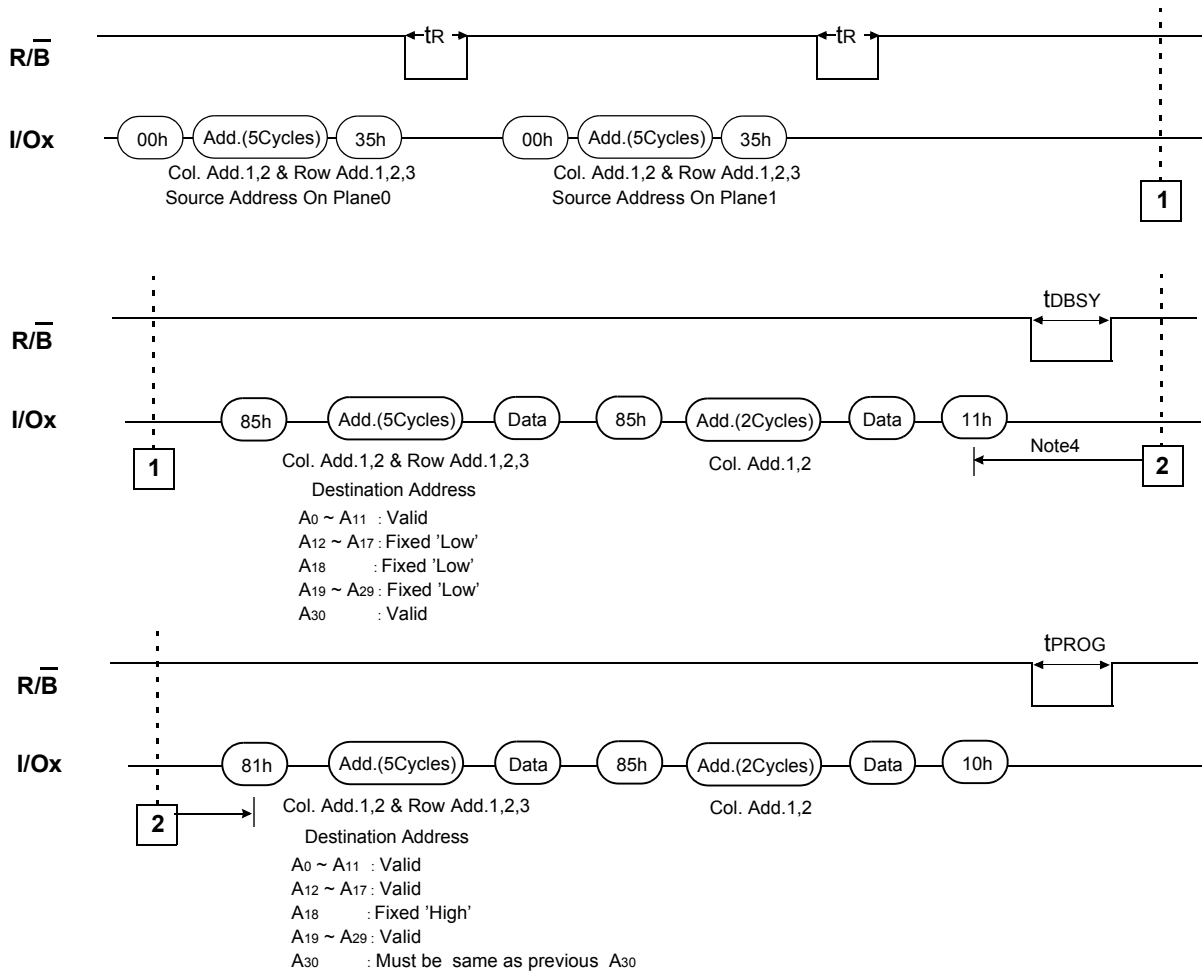
Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 2112 byte page registers. Since the device is equipped with four memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.

Figure 16. Two-Plane Copy-Back Program Operation



- Note:**
- Copy-Back Program operation is allowed only within the same memory plane.
 - On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
 - Two-plane copy-back page program into plane 0&2(or plane 0&3, or plane 1&2, or plane 1&3) is prohibited.
 - Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 17. Two-Plane Copy-Back Program Operation with Random Data Input



- Note:**
- Copy-Back Program operation is allowed only within the same memory plane.
 - On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
 - EDC status Bits are not available during copy back for some bits or bytes modified by Random Data Input operation. In case of the 528 byte plane unit modification, EDC status bits are available.
 - Any command between 11h and 81h is prohibited except 70h and FFh.

READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when $\overline{R/\overline{B}}$ pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to Table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table 3. Status Register Definition for 70h Command

| I/O | Page Program | Block Erase | Read | Definition |
|-------|---------------|---------------|---------------|--|
| I/O 0 | Pass/Fail | Pass/Fail | Not use | Pass : "0" Fail : "1" |
| I/O 1 | Not use | Not use | Not use | Don't -cared |
| I/O 2 | Not use | Not use | Not use | Don't -cared |
| I/O 3 | Not Use | Not Use | Not Use | Don't -cared |
| I/O 4 | Not Use | Not Use | Not Use | Don't -cared |
| I/O 5 | Not Use | Not Use | Not Use | Don't -cared |
| I/O 6 | Ready/Busy | Ready/Busy | Ready/Busy | Busy : "0" Ready : "1" |
| I/O 7 | Write Protect | Write Protect | Write Protect | Protected : "0" Not Protected : "1" |

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
2. Status Register Definition for F1h & F2h command is same as that of 70h command.

READ EDC STATUS

Read EDC status operation is only available on 'Copy Back Program'. The device contains an EDC Status Register which may be read to find out whether there is error during 'Read for Copy Back'. After writing 7Bh command to the command register, a read cycle outputs the content of the EDC Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when $\overline{R/\overline{B}}$ pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in EDC Status Read mode until further commands are issued to it.

Table 4. Status Register Definition for 7Bh Command

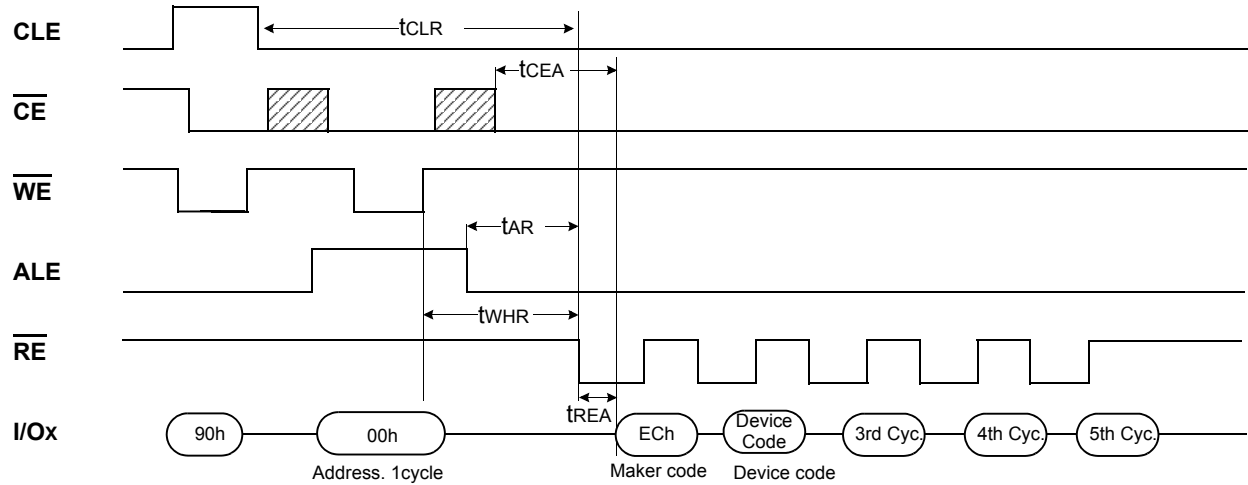
| I/O | Copy Back Program | Page Program | Block Erase | Read | Definition |
|-------|------------------------------------|---------------|---------------|---------------|--------------------------------------|
| I/O 0 | Pass/Fail of Copy Back Program | Pass/Fail | Pass/Fail | Not use | Pass : "0", Fail : "1" |
| I/O 1 | EDC Status | Not use | Not use | Not use | No Error : "0", Error : "1" |
| I/O 2 | Validity of EDC Status | Not use | Not use | Not use | Valid : "1", Invalid : "0" |
| I/O 3 | Not Use | Not Use | Not Use | Not Use | Don't -cared |
| I/O 4 | Not Use | Not Use | Not Use | Not Use | Don't -cared |
| I/O 5 | Not Use | Not Use | Not Use | Not Use | Don't -cared |
| I/O 6 | Ready/Busy of Copy Back Program | Ready/Busy | Ready/Busy | Ready/Busy | Busy : "0", Ready : "1" |
| I/O 7 | Write Protect of Copy Back Program | Write Protect | Write Protect | Write Protect | Protected : "0", Not Protected : "1" |

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
2. More than 2-bit error detection isn't available for each 528 Byte sector.
That is to say, only 1-bit error detection is available for each 528 Byte sector.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 18 shows the operation sequence.

Figure 18. Read ID Operation



| Device | Device Code(2nd Cycle) | 3rd Cycle | 4th Cycle | 5th Cycle |
|------------|--------------------------|-----------|-----------|-----------|
| K9K8G08U0A | D3h | 51h | 95h | 58h |
| K9WAG08U1A | Same as K9K8G08U0A in it | | | |
| K9NBG08U5A | Same as K9K8G08U0A in it | | | |

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when \overline{WP} is high. If the device is already in reset state a new reset command will be accepted by the command register. The $\overline{R/B}$ pin transitions to low for t_{RST} after the Reset command is written. Refer to Figure 19 below.

Figure 19. RESET Operation



Table 5. Device Status

| | After Power-up | After Reset |
|----------------|------------------------|--------------------------|
| Operation mode | 00h Command is latched | Waiting for next command |

READY/BUSY

The device has a $\overline{R/B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The $\overline{R/B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more $\overline{R/B}$ outputs to be Or-tied. Because pull-up resistor value is related to $t_r(\overline{R/B})$ and current drain during busy(i_{busy}), an appropriate value can be obtained with the following reference chart(Fig.20). Its value can be determined by the following guidance.

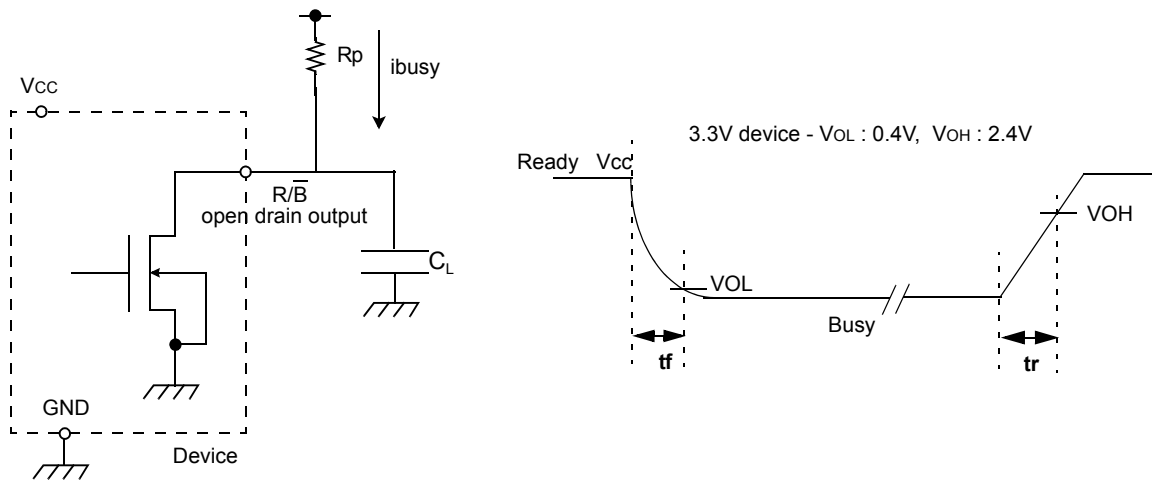
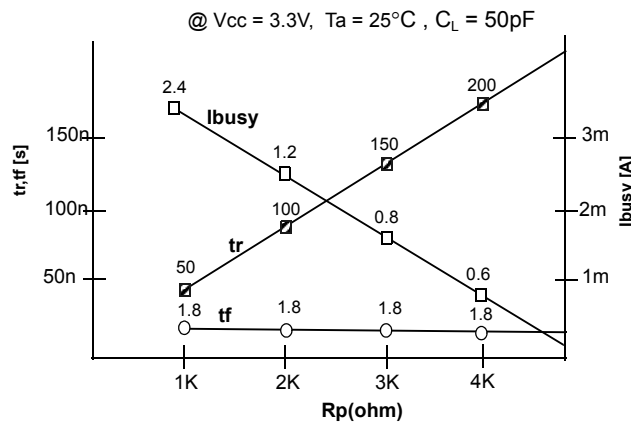


Figure 20. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$R_{p(\min, 3.3V \text{ part})} = \frac{V_{CC(\text{Max.})} - V_{OL(\text{Max.})}}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the $\overline{R/B}$ pin.

$R_{p(\max)}$ is determined by maximum permissible limit of t_r

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V. \overline{WP} pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 100 μ s is required before internal circuit gets ready for any command sequences as shown in Figure 21. The two step command sequence for program/erase provides additional software protection.

Figure 21. AC Waveforms for Power Transition

